DIGITAL IF DEMODULATOR FOR VIDEO APPLICATIONS

5   CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/171,199 filed December 15, 1999, the contents of which is hereby incorporated by reference.

10   BACKGROUND OF THE INVENTION

Intermediate frequency stages ("IF stages") play a key role in a number of applications which require frequency conversion, such as television tuners, set top boxes, and the like. In an exemplary IF stage, a series of signal processing components

15   might be used to convert a signal centered at an IF frequency to a baseband or unmodulated signal suitable for direct extraction its information content.

IF stages typically require filters having frequency selective components that tend to resist integration into an

20   integrated circuit. Other circuits commonly present in an IF stage are oscillators and phase locked loops ("PLLs"). Oscillators often require external crystals or other frequency selective components to form a resonator. PLLs often require an external loop filter. Utilizing digital signal processing

25   techniques would tend to reduce the need for frequency selective components. By sampling an incoming signal and assigning a numerical value to the samples the signal may be processed digitally. After digital processing the numeric values may be converted back to a signal. Digital signal processing techniques

30   tend to allow paramaters, such as pass band characteristics of a filter, to be programmed and otherwise adjusted. Thus, a digital IF providing programmability to accept video signals formatted to various transmission standards can be fabricated.

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Those having skill in the art would understand the desirability of having a digital IF capable of being integrated

5   on an integrated circuit substrate that does not have the problem of requiring a large external component and that may be programmed for multi standard operation. This type of device would necessarily provide a more compact circuit, by having a tunable IF economically integrated onto an integrated circuit.

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SUMMARY OF THE INVENTION

There is therefore provided in a present embodiment of the invention an integrated communications system comprising: a substrate having a receiver disposed on the substrate for

15   converting a received signal to an IF signal, a digital IF demodulator disposed on the substrate and coupled to the receiver for converting the IF signal to a demodulated baseband signal, and a transmitter disposed on the substrate operating in cooperation with the receiver to establish a two way

20   communications path.

Many of the attendant features of this invention will be more readily appreciated as the same becomes better understood by reference to the following detailed description considered in connection with the accompanying drawings.

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DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention will be better understood from the following detailed description read in light of the accompanying drawings, wherein:

FIG. 1 is an illustration of a portion of the over-the-air broadcast spectrum allocations in the United States;

FIG. 2 is an illustration of the frequency spectrum of harmonic distortion products;

FIG. 3 is an illustration of a spectrum of even and odd order intermodulation distortion products;

FIG. 4 is an illustration of interference caused at the IF frequency by a signal present at the image frequency;

FIG. 5 is an illustration of a typical dual conversion receiver utilizing an up conversion and a subsequent down conversion;

OSCILLATOR FIGURES

FIG. 6 is a semi-schematic simplified timing diagram of differential signals, including a common mode component, as might be developed by a differential crystal oscillator in accordance with the invention;

FIG. 7 is a semi-schematic block diagram of a differential crystal oscillator, including a quartz crystal resonator and oscillator circuit differentially coupled to a linear buffer amplifier in accordance with the invention;

FIG. 8 is a simplified schematic illustration of differential signals present at the output of a crystal resonator;

FIG. 9 is a simplified schematic diagram of a quartz crystal resonator equivalent circuit;

FIG. 10 is a simplified graphical representation of a plot of impedance vs. frequency for a crystal resonator operating near resonance;

FIG. 11 is a simplified graphical representation of a plot of phase vs. frequency for a crystal resonator operating near

5   resonance;

FIG. 12 is a simplified schematic diagram of the differential oscillator circuit of FIG. 7;

FIG. 13 is a simplified, semi-schematic block diagram of a periodic signal generation circuit including a crystal oscillator

10   having balanced differential outputs driving cascaded linear and non-linear buffer stages;

FIG. 14 is a simplified schematic diagram of a differential folded cascade linear amplifier suitable for use in connection with the present invention;

15   FIG. 15 is a simplified, semi-schematic diagram of a differential nonlinear buffer amplifier suitable for use as a clock buffer in accordance with the invention;

FIG. 16 is a semi-schematic illustration of an alternative embodiment of the differential oscillator driver circuit;

20   FIG. 17 is an block diagram of a differential crystal oscillator as a reference signal generator in a phase-lock-loop;

FIG. 18 is a simplified block diagram of an illustrative frequency synthesizer that might incorporate the differential periodic signal generation circuit of the invention;

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COARSE/FINE PLL TUNING FIGURES

FIG. 19 is a block diagram illustrating the exemplary frequency conversions for receiver tuning utilized in the embodiments of the invention;

30   FIG. 20 is a block diagram of an exemplary tuner designed to receive a 50 to 860 MHz bandwidth containing a multiplicity of channels;

FIG. 21 is an exemplary table of frequencies utilizing coarse and fine PLL tuning to derive a 44 MHz IF;

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FIG. 22 is an illustration of an alternative embodiment of the coarse and fine PLL tuning method to produce an exemplary
5   final IF of 36 MHz;

FIG. 23 is a block diagram of a dummy component used to model an operative component on an integrated circuit chip;

FILTER TUNING FIGURES

10   FIG. 24a is a block diagram of a tuning process;

FIG. 24b is a flow diagram of the tuning process;

FIG. 24c is an exemplary illustration of the tuning process;

FIG. 25 is a block diagram of an exemplary tuning circuit;

FIG. 26 illustrates the amplitude and phase relationship in
15   an LC filter at resonance;

FIG. 27 is a schematic diagram showing the configuration of switchable capacitors in a differential signal transmission embodiment;

20   ACTIVE FILTER MULTI-TRACK INTEGRATED SPIRAL INDUCTOR FIGURES

FIG. 28a is a plan view of a multi-track spiral inductor suitable for integration onto an integrated circuit, such as one produced with a CMOS process;

FIGS. 28b-28g illustrate various planar devices comprising
25   inductor and transformer configurations suitable for incorporating multiple tracks into their designs;

FIG. 28h is an illustration of a second embodiment of an inductor having a single winding comprising five tracks per layer;

30   FIG. 28i illustrates the placement of tracks in a layered structure;

FIG. 28j is an illustration of an embodiment utilizing a shield disposed beneath an inductor;

FIG. 28k is an illustration of a patterned shield 2864 that
35   is utilized beneath a multi-track inductor;

FIG. 29 is an illustration of the effect of decreasing "Q" on the selectivity of a tuned circuit;

5   FIG. 30 is an illustration of a typical filter bank utilized in embodiments of the invention for filtering I and Q IF signals;

ACTIVE FILTER UTILIZING A LINEARIZED DIFFERENTIAL PAIR AMPLIFIER
10   FIGURES

FIG. 31a is a diagram of an exemplary differential transconductance stage with an LC load;

FIG. 31b is a block diagram of a linearized differential pair amplifier that is coupled to distortion canceling
15   linearization circuit;

FIG. 31c is an illustration depicting a representative channel of any one of the typical field effect of transistors M1, M2, M3, M4;

FIG. 31d is a block diagram showing the interconnection of
20   a differential pair amplifier to a linearization circuit;

FIG. 31e is a schematic illustrating a CMOS differential pair of transistors;

FIG. 31f is a graph of a differential current ($\Delta I_{1,2}=\Delta I_d$) and normalized transconductance (G_m/g_m) as input voltage ($V_i=\Delta V_i$) is
25   varied in the differential pair of FIG. 31e;

FIG. 31g is a schematic diagram of a differential pair amplifier 3127 with a second cross coupled differential pair error amplifier added that tends to reduce distortion;

FIG. 31h is a graph illustrating The linearized output
30   current of a cross coupled differential output amplifier;

FIG. 31i is a schematic of a differential pair amplifier incorporating two auxiliary cross-coupled differential pairs to improve linearization of the output response I_1 and I_2;

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FIG. 31j is a graph of the currents present in the main and two auxiliary differential pair amplifiers graphed against input voltage as measured across the input terminals where $Vin = V_{i1} - V_{i2}$;

FIG. 31k is a graph of transconductance curves for the differential amplifier made up of a main differential pair amplifier 3103 and a linearization circuit comprising differential pair amplifiers;

FIG. 31l illustrates an equivalent circuit that provides an offset voltage V_{os} that permits shaping of The G_m^{Total} curve;

FIG. 31m is a graph of the transconductance curve for The exemplary differential pair amplifier that extends the input voltage range by allowing ripple in the overall G_m of the amplifier;

FIG. 32 shows a transconductance stage with an LC load and Q enhancement;

ACTIVE FILTER INDUCTOR Q TEMPERATURE COMPENSATION FIGURE

FIG. 33 shows a method of tuning inductor Q over temperature;

COMMUNICATIONS RECEIVER FIGURE

FIG. 34 is a block diagram of a communications network utilizing a receiver according to any one of the exemplary embodiments of the invention;

RECEIVER FRONT END-PROGRAMABLE ATTENUATOR AND LNA FIGURES

FIG. 35 is an is an illustration of the input and output signals of the integrated switchless programmable attenuator and low noise amplifier;

FIG. 36 is a functional block diagram of the integrated switchless programmable attenuator and low noise amplifier circuit;

FIG. 37 is a simplified diagram showing the connection of multiple attenuator sections to the output of the integrated

5   switchless programmable attenuator and low noise amplifier;

FIG. 38 is an illustration of an exemplary embodiment showing how the attenuator can be removed from the circuit so that only the LNAs are connected;

FIG. 39 is an attenuator circuit used to achieve one dB per

10   step attenuation;

FIG. 40 is an exemplary embodiment of an attenuator for achieving a finer resolution in attenuation then shown in FIG. 5;

FIG. 41 is an illustration of the construction of series and parallel resistors used in the attenuator circuit of the

15   integrated switchless programmable attenuator and low noise amplifier;

FIG. 42 is an illustration of a preferred embodiment utilized to turn on current tails of the differential amplifiers;

FIG. 43 is an illustration of an embodiment showing how the

20   individual control signals used to turn on individual differential pair amplifiers are generated from a single control signal;

FIGS. 44a and 44b are illustrations of an embodiment of comparator circuitry used to activate individual LNA amplifier

25   stages;

RECEIVER FREQUENCY PLAN AND FREQUENCY CONVERSION
LOCAL OSCILLATOR RELATIONSHIP FIGURE

FIG. 45a is a block diagram illustrating the exemplary

30   generation of the local oscillator signals utilized in the embodiments of the invention;

NARROW BAND PLL2 AND VCO FIGURES

FIG. 45b is a block diagram that illustrates the relation

35   of the VCO to the second LO generation by PLL2.

FIG. 45c is a block diagram of an embodiment of a VCO utilizing a tuning control circuit;

5   FIG. 45d is a block diagram of an embodiment of a VCO utilizing a tuning control circuit showing tuning control circuit interaction with major VCO components;

FIG. 45e is a schematic of a feedback network that allows the frequency of oscillation to be adjusted;

10   FIG. 45f is a schematic of a feedback network that allows the frequency of oscillation to be adjusted by varactor tuning including NMOS devices;

Fig. 45g is a graph of capacitance verses control voltage applied to an NMOS varactor;

15   FIG. 45h is a graph illustrating average capacitance achievable with an NMOS varactor;

FIG. 45i is a schematic of an embodiment of a VCO;

FIG. 45j is a schematic of an equivalent circuit of the VCO of FIG. 45i;

20   FIG. 45k is a schematic of a tuning control circuit controlling switched capacitors to center a varactor tuning range;

FIG. 46a is a schematic of a PLL having its VCO controlled by an embodiment of a VCO tuning control circuit;

25   FIG. 46b illustrates a pulse train output of the phase detector;

NARROW BAND VCO TUNING FIGURES

FIG. 47a is a process flow diagram illustrating the process

30   of tuning the VCO with an embodiment of a VCO control circuit;

FIG. 47b is a flow diagram of a PLL start up and locking process for an embodiment of the invention;

FIG. 47c is a graph of a family of frequency verses control voltage for various capacitor values that illustrates the use of

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comparator hysteresis to aid in achieving a frequency lock
condition;

5   FIG. 47d is a graph of a family of frequency verses control
voltage for various capacitor values that illustrates the use of
dual comparator windows to aid in achieving a frequency lock
condition;

10   RECEIVER FIGURES
        FIG. 48 is a block diagram of the first exemplary embodiment
of the invention;
        FIG. 49 is an illustration of the frequency planning
utilized in the exemplary embodiments of the invention;
15   FIG. 50 is a block diagram showing how image frequency
cancellation is achieved in an I/Q mixer;
        FIG. 51 is a block diagram of the second exemplary
embodiment of the present invention;
        FIG. 52 is a block diagram of the third exemplary embodiment
20   of the present invention;
        FIG. 53 is a block diagram of a CATV tuner that incorporates
the fully integrated tuner architecture;

TELEPHONY OVER CABLE EMBODIMENT FIGURE
25   FIG. 54 is a block diagram of a low power embodiment of the
receiver that has been configured to receive cable telephony
signals.

ELECTRONIC CIRCUITS INCORPORATING EMBODIMENTS OF THE RECEIVER
30   FIGURES
        FIG. 55 is a block diagram of a set top box that
incorporates the receiver embodiments;
        FIG. 56 is a block diagram of a television that incorporates
the receiver embodiments;

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FIG. 57 is a block diagram of a VCR that incorporates the receiver embodiments;

5   FIG. 58 is a block diagram of a cable modem that incorporates the integrated switchless programmable attenuator and low noise amplifier;

ESD PROTECTION FIGURES

10   FIG. 59 is an illustration of a typical integrated circuit die layout;

FIG. 60 illustrates an embodiment of the invention that utilizes pad ring power and ground busses;

FIG. 61 is an illustration of the connection of a series of

15   power domains to a pad ring bus structure;

FIG. 62 is an illustration of an embodiment utilizing an ESD ground ring;

FIG. 63 is an illustration of the effect of parasitic circuit elements on an RF input signal;

20   FIG. 64 illustrates a cross-talk coupling mechanism;

FIG. 65 is an illustration of an ESD device disposed between a connection to a bonding pad and power supply traces;

FIG. 66 is an illustration of parasitic capacitance in a typical bonding pad arrangement on an integrated circuit;

25   FIG. 67 is an illustration of a embodiment of a bonding pad arrangement tending to reduce parasitic capacitances;

FIG. 68 illustrates a cross section of the bonding pad structure of FIG. 67;

FIGS. 69a-69e illustrate various ESD protection schemes

30   utilized in the state of the art to protect an integrated circuit from ESD discharge due to charge build up on a die pad;

FIG. 70 illustrates an approach to pad protection during ESD event;

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FIG. 71 is a schematic of a circuit immune to noise that uses an ggNMOS' C_{gd} and a gate boosting structure to trigger ESD

5   protection;

FIG. 72 is a schematic of an alternative embodiment utilizing the gate boosting structure and a cascode configuration; and

FIG. 73 is a schematic of an embodiment that does not

10   require a quiet power supply.

IF AGC AMPLIFIER FIGURES

FIG. 74 is a block diagram of a variable gain amplifier ("VGA");

15   FIG. 75, is a block diagram of the internal configuration of the VGA and the linearization circuit;

FIG. 76 is a graph of gain versus the control current iSig. Control current iSig is shown as a fraction of iAtten, with the total current being equal to 1, or 100%;

20   FIG. 77 is the schematic diagram of an embodiment of the VGA. The VGA has a control circuit to control the V_{ds} of M10 and M13 at node 7505, and the V_{ds} of M4 and M14 at node 7507;

FIG. 78a illustrates a family of curves showing the relationship of a transistor's drain current ("I_d") to its gate

25   source voltage ("V_{gs}") measured at each of a series of drain source voltages ("V_{ds}") from 50 mV to 1 V;

FIG. 78b is a graph of g_m verses V_{gs} as V_{ds} is varied from 50 mV to 1 V;

FIG. 78c is a graph of the cross-section of FIG. 78b

30   plotting g_m verses V_{ds} for various values of V_{gs};

FIG. 79 is a schematic of a current steering circuit;

FIG. 80 is a schematic of a VD1 control signal generation circuit.

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DIGITAL IF DEMODULATOR FIGURES

FIG. 81 is an is a block diagram of a typical prior art IF demodulator;

FIG. 82 is a frequency spectrum of a typical NTSC television signal;

FIG. 83 is a block diagram of an embodiment of a digital IF demodulator;

FIGS. 84a-84d are frequency spectra showing digital VIF demodulation and Nyquist filtering of an exemplary received band of television channels received at an IF frequency and presented to the VIF demodulator and Nyquist filter and the circuitry contained therein;

FIG. 85 is a spectrum of an NTSC television signal relative to the filter responses of filters 8327, 8337 and 8345;

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is an illustration of a portion of the radio frequency spectrum allocations by the FCC. Transmission over a given media occurs at any one of a given range of frequencies that are suitable for transmission through a medium. A set of frequencies available for transmission over a medium are divided into frequency bands 102. Frequency bands are typically allocations of frequencies for certain types of transmission. For example FM radio broadcasts, FM being a type of modulation, is broadcast on the band of frequencies from 88 MHz to 108 MHz 104. Amplitude modulation (AM), another type of modulation, is allocated the frequency band of 540 kHz to 1,600 kHz 106. The frequency band for a type of transmission is typically subdivided into a number of channels. A channel 112 is a convenient way to refer to a range of frequencies allocated to a single broadcast station. A station broadcasting on a given channel may transmit one or more radio frequency (RF) signals within this band to convey the information of a broadcast. Thus, several frequencies

transmitting within a given band may be used to convey information from a transmitter to a broadcast receiver. For
5   example, a television broadcast channel broadcasts its audio signal(s) 108 on a frequency modulated (FM) carrier signal within the given channel. A TV picture (P) 110 is a separate signal broadcast using a type of amplitude modulation (AM) called vestigial side band modulation (VSB), and is transmitted within
10   this channel.

In FIG. 1 channel allocations for a television broadcast band showing the locations of a picture and a sound carrier frequencies within a channel are shown. Each channel 112 for television has an allocated fixed bandwidth of 6 MHz. The
15   picture 110 and sound 108 carriers are assigned a fixed position relative to each other within the 6 MHz band. This positioning is not a random selection. The picture and sound carriers each require a predetermined range of frequencies, or a bandwidth (BW) to sufficiently transmit the desired information. Thus, a
20   channel width is a fixed 6 MHz, with the picture and sound carrier position fixed within that 6 MHz band, and each carrier is allocated a certain bandwidth to transmit its signal.

In FIG. 1 it is seen that there are gaps between channels 114, and also between carrier signals 116. It is necessary to
25   leave gaps of unused frequencies between the carriers and between the channels to prevent interference between channels and between carriers within a given channel. This interference primarily arises in the receiver circuit that is used to receive these radio frequency signals, convert them to a usable frequency, and
30   subsequently demodulate them.

Providing a signal spacing allows the practical design and implementation of a receiver without placing unrealistic requirements on the components in the receiver. The spaces help prevent fluctuations in the transmission frequency or spurious
35   responses that are unwanted byproducts of the transmission not

to cause interference and signal degradation within the receiver.
Also, signal spacing allows the design requirements of frequency
5   selective circuits in the receiver to be relaxed, so that the
receiver may be built economically while still providing
satisfactory performance.   These spectrum allocations and
spacings were primarily formulated when the state of the art in
receiver design consisted of discrete components spaced
10   relatively far apart on a printed circuit board. The increasing
trend towards miniaturization has challenged these earlier
assumptions. The state of the art in integrated circuit receiver
design has advanced such that satisfactory performance must be
achieved in light of the existing spectrum allocations and
15   circuit component crowding on the integrated circuit. New ways
of applying existing technology, as well as new technology are
continually being applied to realize a miniaturized integrated
receiver that provides satisfactory performance. Selectivity is
a principal measure of receiver performance.   Designing for
20   sufficient selectivity not only involves rejecting other
channels, but the rejection of distortion products that are
created in the receiver or are part of the received signal.
Design for minimization or elimination of spurious responses is
a major objective in state of the art receiver design.

25   FIG. 2 is an illustration of harmonic distortion products.
Transmitted spurious signals, and spurious signals generated in
a receiver, most commonly consist of harmonics created by one
frequency and intermodulation distortion, created by the
interaction of multiple frequencies. Spurious signals at other
30   than the desired frequency arise from the inherent nonlinear
properties in the circuit components used. These nonlinearities
can not be eliminated, but by careful engineering the circuitry
can be designed to operate in a substantially linear fashion.

When a single frequency called a fundamental 202 is
35   generated, unwanted spurious signals 204 are always generated

with this fundamental. The spurious signals produced as a result of generating a single frequency (f) 202 are called harmonics 204

5   and occur at integer multiples of the fundamental frequency (2f, 3f, ...) The signal strength or amplitude of these harmonics decrease with increasing harmonic frequency. Fortunately these distortion products fall one or more octaves away from the desired signal, and can usually be satisfactorily filtered out

10   with a low pass filter that blocks all frequencies above a pre-selected cut-off frequency. However, if the receiver is a wide band or multi octave bandwidth receiver, these harmonics will fall within the bandwidth of the receiver and cannot be low pass filtered, without also filtering out some of the desired signals.

15   In this case, other methods known to those skilled in the art, such as reducing the distortion products produced, must be used to eliminate this distortion.

Radio signals do not exist in isolation. The radio frequency spectrum is populated by many channels within a given

20   band transmitting at various frequencies. When a radio circuit is presented with two or more frequencies, these frequencies interact, or intermodulate, to create distortion products that occur at known frequency locations.

FIG. 3 is an illustration of intermodulation distortion

25   products. Whenever two or more frequencies are present they interact to produce additional spurious signals that are undesired. FIG. 3 illustrates a spurious response produced from the interaction of two signals, f_1 302 and f_2 304. This particular type of distortion is called intermodulation

30   distortion (IMD). These intermodulation distortion products 306 are assigned orders, as illustrated. In classifying the distortion the IM products are grouped into two families, even and odd order IM products. Odd order products are shown in FIG. 3.

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In a narrow band systems the even order IM products can be easily filtered out, like harmonics, because they occur far from the two original frequencies. The odd order IM products 306 fall close to the two original frequencies 302, 304. In a receiver these frequencies would be two received signals or a received channel and a local oscillator. These products are difficult to remove. The third order products 306 are the most problematic in receiver design because they are typically the strongest, and fall close within a receiver's tuning band close to the desired signal. IM distortion performance specifications are important because they are a measure of the receiver's immunity to strong out of band signal interference.

Third order products 308 occur at $(f_1 - \Delta f)$ and at $(f_2 + \Delta f)$, where $\Delta f = f_2 - f_1$. These unwanted signals may be generated in a transmitter and transmitted along with desired signal or are created in a receiver. Circuitry in the receiver is required to block these signals. These unwanted spurious responses arise from nonlinearities in the circuitry that makes up the receiver.

The circuits that make up the receiver though nonlinear are capable of operating linearly if the signals presented to the receiver circuits are confined to signal levels within a range that does not call for operation of the circuitry in the nonlinear region. This can be achieved by careful design of the receiver.

For example, if an amplifier is over driven by signals presented to it greater than it was designed to amplify, the output signal will be distorted. In an audio amplifier this distortion is heard on a speaker. In a radio receiver the distortion produced in nonlinear circuits, including amplifiers and mixers similarly causes degradation of the signal output of the receiver. On a spectrum analyzer this distortion can be seen; levels of the distortion increase to levels comparable to the desired signal.

While unwanted distortion such as harmonic distortion, can
be filtered out because the harmonics most often fall outside of
5   the frequency band received, other distortion such as inter-
modulation distortion is more problematic. This distortion falls
within a received signal band and cannot be easily filtered out
without blocking other desired signals. Thus, frequency planning
is often used to control the location of distortion signals that
10   degrade selectivity.

Frequency planning is the selection of local oscillator
signals that create the intermediate frequency (IF) signals of
the down conversion process. It is an analytical assessment of
the frequencies being used and the distortion products associated
15   with these frequencies that have been selected. By evaluating
the distortion and its strength, an engineer can select local
oscillator and IF frequencies that will yield the best overall
receiver performance, such as selectivity and image response.
In designing a radio receiver, the primary problems encountered
20   are designing for sufficient sensitivity, selectivity and image
response.

Selectivity is a measure of a radio receiver's ability to
reject signals outside of the band being tuned by a radio
receiver. A way to increase selectivity is to provide a resonant
25   circuit after an antenna and before the receiver's frequency
conversion circuitry in a "front end." For example, a parallel
resonant circuit after an antenna and before a first mixer that
can be tuned to the band desired will produce a high impedance
to ground at the center of the band. The high impedance will
30   allow the antenna signal to develop a voltage across this
impedance. Signals out of band will not develop the high voltage
and are thus attenuated.

The out of band signal rejection is determined by a quality
factor or "Q" of components used in the resonant circuit. The
35   higher the Q of a circuit in the preselector, the steeper the

slope of the impedance curve that is characteristic of the
preselector will be. A steep curve will develop a higher voltage
5   at resonance for signals in band compared to signals out of band.
For a resonant circuit with low Q a voltage developed across the
resonant circuit at a tuned frequency band will be closer in
value to the voltage developed across the resonant circuit out
of band. Thus, an out of band signals would be closer in
10   amplitude to an in band signals than if a high Q circuit were
constructed.

 This type of resonant circuit used as a preselector will
increase frequency selectivity of a receiver that has been
designed with this stage at its input.   If an active preselector
15   circuit is used between an antenna and frequency conversion
stages, the sensitivity of the receiver will be increased as well
as improving selectivity. If a signal is weak its level will be
close to a background noise level that is present on an antenna
in addition to a signal. If this signal cannot be separated from
20   the noise, the radio signal will not be able to be converted to
a signal usable by the receiver. Within the receiver's signal
processing chain, the signal's amplitude is decreased by losses
at every stage of the processing. To make up for this loss the
signal can be amplified initially before it is processed. Thus,
25   it can be seen why it is desirable to provide a circuit in the
receiver that provides frequency selectivity and gain early in
the signal processing chain.

 Radio frequency tuners are increasingly being designed with
major portions of their circuitry implemented as an integrated
30   circuit. In the state of the art to minimize distortion products
created in the receiver, exotic materials such as gallium
arsenide (GaAs) are used. A receiver implemented on this type
of material will typically have lower distortion and noise
present than in a similarly constructed receiver constructed on
35   silicon. Silicon, is an attractive material due to its low cost.

In addition, a CMOS circuit implemented on silicon has the additional benefit of having known processing characteristics that allow a high degree of repeatability from lot to lot of wafers.   The state of the art has not achieved a completely integrated receiver in CMOS circuitry. A reason for this is the difficulty of eliminating receiver distortion and noise.

The distortion products discussed above that are created in the receiver can, in the majority of cases, also be reduced by setting an appropriate drive level in the receiver, and by allowing a sufficient spacing between carriers and channels. These receiver design parameters are dependent upon many other factors as well, such as noise present in the system, frequency, type of modulation, and signal strength among others. Noise is one of the most important of these other parameters that determines the sensitivity of the receiver, or how well a weak signal may be satisfactorily received.

Noise is present with the transmitted signal, and also generated within a receiver. If excessive noise is created in a receiver a weak signal may be lost in a "noise floor". This means that the strength of the received signal is comparable to the strength of the noise present, and the receiver is incapable of satisfactorily separating a signal out of this background noise, or floor. To obtain satisfactory performance a "noise floor" is best reduced early in a receiver's chain of circuit components.

Once a signal is acquired and presented to a receiver, in particularly an integrated receiver with external pins, additional noise may be radiated onto those pins.   Thus, additional added noise at the receiver pins can degrade the received signal.

In addition to the noise that is present on an antenna or a cable input to a receiver, noise is generated inside the radio receiver.   At a UHF frequency range this internal noise

predominates over the noise received with the signal of interest.
Thus, for the higher frequencies the weakest signal that can be
5   detected is determined by the noise level in the receiver. To
increase the sensitivity of the receiver a "pre-amplifier" is
often used after an antenna as a receiver front end to boost the
signal level that goes into the receiver. This kind of pre-
amplification at the front end of the amplifier will add noise
10   to the receiver due to the noise that is generated inside of this
amplifier circuit. However, the noise contribution of this
amplifier can be minimized by using an amplifier that is designed
to produce minimal noise when it amplifies a signal, such as an
LNA. Noise does not simply add from stage to stage; the internal
15   noise of the first amplifier substantially sets the noise floor
for the entire receiver.

In calculating a gain in a series of cascaded amplifiers the
overall gain is simply the sum of the gains of the individual
amplifiers in decibels. For example, the total gain in a series
20   of two amplifiers each having a gain of 10 dB is 20 dB for a
overall amplifier. Noise floor is commonly indicated by the
noise figure (NF). The larger the NF the higher the noise floor
of the circuit.

A cascaded noise figure is not as easily calculated as
25   amplifier gain; its calculation is non-intuitive. In a series
of cascaded amplifiers, gain does not depend upon the positioning
of the amplifiers in the chain. However, in achieving a given
noise figure for a receiver, the placement of the amplifiers is
critical with respect to establishing a receiver's noise floor.
30   In calculating the noise figure for an electronic system Friis'

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equation is used to calculate the noise figure of the entire system. Friis' equation is:

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$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots + \frac{NF_n - 1}{G_1 G_2 \ldots G_n} \tag{1}$$

NF_{total} = system noise figure

10   NF_1 = noise figure of stage-1

NF_2 = noise figure of stage-2

NF_n = noise figure of stage-nth

G_1 = gain of stage-1

G_2 = gain of stage-2

15   G_N = gain of nth stage

What can be seen from this equation is that the noise figure of a first stage is the predominant contributor to a total noise figure. For example, the noise figure of a system is only

20   increased a small amount when a second amplifier is used. Thus, it can be seen that the noise figure of the first amplifier in a chain of amplifiers or system components is critical in maintaining a low noise floor for an entire system or receiver. A low NF amplifier typically requires a low noise material for

25   transistors, such as gallium arsenide. Later amplifiers that do not contribute significantly to the noise, are constructed of a cheaper and noisier material such as silicon.

The initial low noise amplifiers are typically constructed from expensive materials such as gallium arsenide to achieve

30   sufficient performance.   Gallium arsenide requires special processing, further adding to its expense. Additionally, GaAs circuits are not easily integrated with silicon circuits that make up the bulk of the receivers in use. It would be desirable to achieve identical performance with a less costly material,

35   such as silicon.   Silicon requires less costly processing.

Further it is advantageous if a standard process, such as CMOS, could be used to achieve the required low noise design. Given

5   the trend towards miniaturization and high volume production, it is highly desirable to be able to produce an integrated receiver with a low noise floor on silicon.

Within a receiver the layout and spacing of circuitry is critical to avoid the injection of noise generated in other

10   portions of the circuit onto a received signal. If a tuner is placed on a semiconductor substrate noise generated in the substrate itself will interfere with, and degrade the received signal, this has been a problem preventing complete integration of a receiver on silicon.

15   Historically low noise substrates, fabricated from exotic and costly materials such as gallium arsenide have been used to reduce noise generated by the semiconductor substrate. However, it would be advantageous to be able to fabricate a receiver on a single CMOS substrate. CMOS advantageously is a known process

20   that may be implemented economically for volume production. Currently a receiver fabricated completely in CMOS has not been available without utilizing external components in the received signal path. Each time the signal is routed on or off of the integrated circuit additional opportunities for the introduction

25   of noise into a signal path are provided. Minimizing this introduction of noise is an ongoing problem in receiver design.

After preselection and low noise amplification that is performed in a front end of a receiver, the signal next enters the receiver's frequency conversion circuitry. This circuitry

30   takes channels that have been passed through the front end and converts one of the selected channel's frequencies down to one or more known frequencies (f_{IF} or IFs). This frequency conversion is accomplished through the use of a circuit called a mixer that utilizes a local oscillator signal (f_{LO}), usually

35   generated in the receiver, to tune a received channel to an IF

frequency while blocking the other channels. Spurious signals, previously described, are produced in this receiver circuitry, and an additional problem known as "image response" is encountered that must be considered in the receiver's design.

It is well known to those skilled in the art that when two sinusoidal signals of differing frequencies are multiplied together by their application to a nonlinear device, such as a mixer, that signals of a differing frequency are produced. A mixer has three ports: f_{RF} receives a low level radio frequency signal that contains the desired modulation, f_{LO} is a high level signal from a local oscillator, and f_{IF} is the resultant mixer product or intermediate frequency produced. These frequencies are related:

$$f_{IF} \quad = \quad mf_{RF} \pm nf_{LO} \tag{2}$$
$$\text{where } m=0, \ 1, \ 2, \ 3, \ \ldots \text{ and}$$
$$n=0, \ 1, \ 2, \ 3, \ \ldots$$

In a typical first order circuit (m=n=1) four frequencies are produced: f_{RF}, f_{LO}, $f_{IFLO}=f_{RF}-f_{LO}$ and $f_{IFHI}=f_{RF}+f_{LO}$. A f_{IFLO} and f_{IFHI} being termed intermediate frequencies. In receivers the common practice is to select either the sum or difference IF frequency by filtering out the undesired one. Since both signals contain the same information, only one is needed in the subsequent circuitry.

One or more mixers are advantageously used in radio receivers to convert a high frequency radio signal which is received into a lower frequency signal that can be easily processed by subsequent circuitry. Mixers are also used to tune multiple channels, so that different tuned circuits are not required for each channel. By changing a local oscillator frequency, differing radio frequencies received can be tuned to produce a constant intermediate frequency value regardless of the

frequency of the received channel. This means that circuit components used to process the intermediate frequency may be

5   fixed in value, with no tuning of capacitors or coils required. Thus, circuits in an IF strip are all fixed-tuned at an IF frequency. A receiver constructed in this manner, using one or more frequency conversions, is called a superheterodyne radio receiver.

10   A disadvantage of a superheterodyne radio receiver is that any of the one or more local oscillators within the receiver also acts as a miniature transmitter. A receiver "front end" alleviates this problem by isolating an antenna from the remaining receiver circuitry.

15   By positioning a radio frequency amplifier between the antenna and the frequency converting stages of a receiver, additional isolation between the receiver circuitry and the antenna is achieved. The presence of an amplifier stage provides attenuation for any of the one or more local oscillator signals

20   from the frequency conversion stages that are radiated back towards the antenna or a cable distribution network. This increased isolation has the benefit of preventing radiation of a local oscillator signal out the antenna which could cause radio frequency interference from a local oscillator. If radiated

25   these and other signals present could create interference in another receiver present at another location.

FIG. 4 is an illustration that shows an image frequency's 402 relation to other signals present 404, 406, 408 at a mixer. Image frequency suppression is an important parameter in a

30   receivers design. In a radio receiver two frequencies input to a radio receiver 404, 406 will yield a signal at the IF frequency 408. A receiver will simultaneously detect signals at the desired frequency 404 and also any signals present at an undesired frequency known as the image frequency 402. If there

35   is a signal present at the image frequency, it will translate

down to the IF frequency 408 and cause interference with the
reception of the desired channel. Both of these signals will be
5   converted to the IF frequency unless the receiver is designed to
prevent this. The image frequency 402 is given by:

$$f_I = f_{RF} + 2f_{IF} \qquad\qquad (3)$$

10   where f_I is the image frequency. This is illustrated in FIG. 4.
A frequency that is spaced the IF frequency 410 below the local
oscillator frequency (f_{RF}) 404, and a frequency that is spaced
the intermediate frequency 412 above the local oscillator signal
(f_-) 402, will both be converted down to the intermediate
15   frequency (f_{IF}) 408. The usual case is that a frequency that
occurs lower than the local oscillator signal is the desired
signal. The signal occurring at the local oscillator frequency
plus the intermediate frequency 402 is an unwanted signal or
noise at that frequency that is converted to the IF frequency
20   causing interference with the desired signal.

In FIG. 4 the exemplary 560 KHz signal 404 is a radio
station that the tuner is tuned to receive. The exemplary
1470 KHz signal 402 is another radio station transmitting at that
particular frequency. If a designer of the receiver had picked
25   an exemplary local oscillator signal of 1015 KHz 406 then both
of these radio stations would be simultaneously converted to an
exemplary IF frequency of 455 KHz 408. The person listening to
the radio would simultaneously hear both radio programs coming
out of his speaker. This illustrates the need for the careful
30   selection of local oscillator frequencies when designing a radio
receiver. The selection of local oscillator frequencies is a
part of frequency planning and used by those skilled in the art
to aesign a receiver that will provide frequency conversions
needed with minimal distortion.

35

FIG. 5 illustrates a dual (or double) conversion receiver 502. Such a multiple conversion receiver allows selectivity, distortion and stability to be controlled through a judicious frequency planning. In the double conversion receiver 502 a received signal 504 is first mixed 506 to a first intermediate frequency, and then mixed 508 down to a second intermediate frequency. In this type of receiver the first IF frequency is made to be high so that a good image rejection is achieved. The second IF is made low so that good adjacent channel selectivity is achieved.

If the first IF frequency is low an image frequency falls higher in frequency, or closer to the center of a pass band of an RF selectivity curve of a receiver "front end," 510 and undergoes little attenuation. If the IF frequency is high the image frequency falls far down on the skirt of the RF selectivity curve for the receiver "front end" receiving a required attenuation. Thus, the selectivity of the receiver acts to attenuate the image frequency when a high IF frequency is used. As an added benefit a high image frequency provides less of a chance for interference from a high powered station. This is because at higher frequencies transmitted power is often lower due to the difficulties in generating RF power as frequency increases.

A low second IF frequency produces a good adjacent channel selectivity. Frequency spacing between adjacent channels is fixed. To prevent interference from adjacent channels the receiver must possess a good selectivity. Selectivity can be achieved through a RF tuned circuit, and more importantly by the superior selectivity provided by a frequency conversion process. The selectivity improvement given by using a low IF is shown by considering a percent separation of a desired and an undesired signal relative to total signal bandwidth. If a separation between the desired and undesired signals is constant a second

IF signal falling at the lower frequency will give a larger
percent separation between the signals. As a result it is easier
5   to distinguish between IF signals that are separated by a larger
percentage of bandwidth. Thus, the judicious selection of two
intermediate frequencies in a double conversion receiver is often
used to achieve a given design goal, such as image frequency
rejection and selectivity.

10   Additionally, the use of a second IF frequency allows gain
in the receiver to be distributed evenly. Distributing gain
helps prevent instability in the receiver. Instability usually
is seen as an oscillating output signal 512. Distributing the
gain among several IF amplifiers 514, 516, 518 reduces the chance
15   of this undesirable effect. Often to further distribute the gain
required in a system design a third frequency conversion, and a
third IF frequency, will be utilized.

          After a receiver front end that possibly contains a low
noise amplifier, additional amplifiers are often seen in the
20   various IF strips. An amplifier in an IF strip does not require
frequency tuning and provides signal gain to make up for signal
losses, encountered in processing a received signal. Such losses
can include conversion loss in mixers and the insertion loss
encountered by placing a circuit element, such as a filter or an
25   isolator in the IF strip.

          In receivers filters are used liberally to limit unwanted
frequencies that have been escaped previous elimination in a
"front end," or to eliminate unwanted frequencies that have been
created immediately preceding a filter. In addition to
30   attenuating unwanted frequencies, a desired signal will also
undergo some attenuation. This attenuation results from an
insertion loss of a filter, or some other component, and if
uncompensated, will degrade a signal. This is especially true
when a series of filters are cascaded, since the effect is
35   additive.

Often a series of multiple filters are cascaded in a given IF strip. These filters typically have an identical response

5   characteristic. The cascaded filters are used to increase the selectivity of the receiver. While it is true that the insertion loss in the pass band is the sum of individual filter insertion losses, as measured in decibels, a rejection improvement obtained outside of the pass band is the sum of the rejections at the

10   given frequency. Thus, three cascaded filters, each having an insertion loss of .01 dB at a center frequency, would have a total insertion loss of .03 dB. If the rejection in the stop band, a given frequency away from the center frequency of the filter, were 20 dB, then a total rejection for 3 cascaded filters

15   would be 60 dB, a great improvement in filter selectivity.

In choosing intermediate frequencies for IF strips in the receiver, no concrete design guidelines exist. Also because of a wide variance in design goals that are encountered in receiver design, concrete methodologies do not exist. Each receiver must

20   be uniquely engineered to satisfy a series of system design goals taking into consideration design tradeoffs that must be made. In the current state of the art, design tradeoffs, and design methodologies used have been directed to integrating all parts of the receiver except for frequencies selective components. The

25   conventional wisdom in receiver design is that filters are not easily integrated onto a silicon substrate and that filtering is best done off of a chip.

Some general design guidelines exist to aid an RF engineer in designing a receiver. One such rule is that designing for

30   receiver selectivity is more important than designing for receiver sensitivity. Thus, when faced with conflicting design choices, the more desirable choice is to provide a design that will separate adjacent channels that interfere with each other rather than to design a receiver capable of picking up the

35   weakest channels. Another rule of thumb in choosing intermediate

frequencies is to choose the first intermediate frequency at
twice the highest input frequency anticipated. This is to reduce
5   the possibility of spurious second order intermodulation
distortion. Depending upon a system performance desired, this
rule can even be more restrictive, requiring an IF at greater
than three times the highest input frequency. Thus, it may be
seen that a wide variety of performance requirements exist in a
10 receiver circuit, and that the range of choices for a given
criteria may be utilized by those skilled in the art to produce
a unique design that meets the challenges posed by an increasing
trend towards integration.

When more than one IF is present in a receiver there is an
15 image frequency associated with each IF that must be considered
in the design. A good receiver provides an image rejection
greater than 70 dB.

One of the first considerations in frequency planning a
superheterodyne receiver is the selection of IF conversions. A
20 frequency range of the local oscillator needs to be determined
to establish the locations of spurious responses of various
orders. Two choices are possible for each of two possible LO
frequency and the selection is not subject to an easy
generalization. The two available frequencies are the absolute
25 value of the quantity $|f_{RF}\pm f_{IF}|=f_{LO}$. Selection depends on RF bands
chosen to be received and frequencies present in these bands, the
availability of fixed bandwidth filters at a desired IF and
constraints imposed upon an engineer by the limitations of a
material that will be used to fabricate a receiver.

30 Receiver planning is a process that is centered upon
frequency planning and receiver level diagrams. After initial
frequency selections for a frequency plan are made, a receiver
level plan is used to calculate noise figures, intercept points
(IP) and levels of spurious responses. Each is evaluated in
35 light of design requirements. After each set of selections

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performance is evaluated and a next set of parameter selections is made until an appropriate compromise in receiver performance

5   is achieved.

Once frequency planning and a level diagram yield a satisfactory design solution these tools are used to guide a detailed receiver design. Once parameters of a section of a receiver are defined, an engineer can use various circuit

10   implementations to achieve a stated design goal. For example a frequency plan and level diagram may require a band pass filter with certain characteristics such as bandwidth, center frequency and insertion loss. The engineer would then either pick a single filter that meets all of these requirements or cascade one or

15   more filters such that a composite response will yield the required design value.

Needless to say experience and knowledge of available technology plays a large part in achieving a successful receiver design blueprint. An engineer must have a rough idea of

20   component availability and design methodologies that will yield a certain performance. If the engineer specifies a portion of the receiver that has performance characteristics that are not achievable with available components or design methods, then an impractical and unproduceable design has been proposed requiring

25   replanning the architecture of the receiver.

A design process and a result achieved is very dependent upon technology available, materials and methodologies known at the time. New improvements in design techniques, computer simulation, processing and a push for increased miniaturization

30   continually fuel achievement of new and innovative receiver designs to solve technological problems.

Once frequency conversions have been chosen and a receiver designed, with the distortion products created in the receiver found acceptable, the next step in receiver design is to design

35   circuitry that will generate one or more local oscillator

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signals. These signals could be provided by a source that is external to a chip. However, this would not be practical in
5   seeking to miniaturize an overall receiver design. A better approach is to generate the local oscillator frequencies near the receiver. In reducing an entire receiver onto a single chip, problems in maintaining signal purity, and stability are encountered.

10   An innovation that has allowed increased miniaturization in receiver design is the development of frequency synthesis. Local oscillator signals are required in receivers utilizing frequency conversion. These signals must be tunable and stable. A stable frequency is easily produced by a quartz crystal at a single
15   frequency. A tunable frequency can be produced by an LC type oscillator. However, this LC oscillator does not have sufficient stability. Additionally using a large number of crystals to generate a range of local oscillator signals, or inductors required in an LC oscillator do not allow an easily miniaturized
20   design. Frequency synthesis is space efficient.

Variable frequency local oscillator signals used in a receiver must be generated by appropriate circuits. These frequency synthesis techniques derive variable LO signals from a common stable reference oscillator. A crystal oscillator has
25   a stable frequency suitable for use in a synthesizer.

Oscillators may provide a fixed or a variable output frequency. This fixed or variable frequency may be used for frequency conversion in a receiver as a local oscillator that is used to mix a received radio frequency (RF) input down to an
30   intermediate frequency or a base band signal that is more easily processed in the following circuitry. Another way that a received signal can be converted down to a base band or intermediate frequency signal is by using frequency synthesizer outputs as local oscillator signals to mix the signal down.
35   Synthesizers provide accurate, stable and digitally programmable

frequency outputs, without the use of multiple oscillators to tune across a band. Accuracy is maintained by using feed back.

5   Three general techniques are used for frequencies synthesis. Direct synthesizers use frequency multipliers, dividers and mixers. Indirect synthesizers use phase-locked loops. Direct digital synthesizers use digital logic combined with a digital to analog converter to provide an analog output. Some designs

10 combine the three techniques.

A direct synthesizer will use a frequency reference such as a crystal oscillator as disclosed in FIG. 5 to generate a reference frequency. To achieve a desired output frequency, the reference frequency is multiplied through a series of

15 multipliers. Dividers may be used similarly to reduce the frequency output to the desired lesser value. Additionally, two signals generated from the chain of multipliers and dividers can be fed into a mixer to generate a third frequency. The mix and divide direct synthesis approach permits the use of many

20 identical modules that produce fine resolution with low spurious output.

Indirect synthesis can take several forms. It can use divide by N to produce one or more of the digits, and mix and divide with loops imbedded among circuits. In each form of

25 frequency synthesizer, the loops contained in it are governed by a derivative of a reference frequency. Indirect synthesis can be used to generate a frequency of $\left(\dfrac{N}{M}\right)f_{in}$. Circuits of this type are often used as local oscillators for digitally tuned radio and television receivers.

30   Indirect synthesizers make use of a number of phase locked loops (PLLs) in order to create a variety of frequency outputs. Each loop present in the system makes use of a common frequency reference provided by a single oscillator. Frequency synthesizers provide the advantage of being digitally programmable to a

35

desired frequency as well as providing an extremely stable frequency.

5   Frequency stability in a synthesizer is achieved with phase locked loops. A phase locked loop is programmed to generate a desired frequency. Once it approximates the frequency, the frequency is divided down to the value of a reference frequency, provided by an external oscillator, and compared to that

10   reference frequency. When the difference reaches zero the phase locked loop stops tuning and locks to the frequency that it has just produced. The frequency reference used to tune the phase locked loop is typically provided by a single frequency oscillator circuit.

15   Frequency synthesizers in a radio frequency receiver often incorporate two phase locked loops. One PLL is used to provide coarse tuning within the frequency band of interest while the second PLL provides fine tuning steps.

           In using this scheme, a coarse tuning must be such that a

20   desired channel will initially fall within the selectivity of the receiver to produce a signal output. It would be an advantage in receiver design if tuning speed could be increased so that initially several channels would fall within the selectivity of the receiver. Tuning in this manner would allow an output to be

25   created with an extremely coarse tuning range that could be dynamically adjusted. Currently this type of tuning is not seen in the state of the art.

           Typically PLLs use a common reference frequency oscillator. Local oscillator signals produced by a frequency synthesizer's

30   phase locked loops inject noise produced in the reference frequency oscillator and the PLLs into a the signal path by way of a PLL output.

           A range of output frequencies from a synthesizer can span many decades, depending on the design. A "resolution" of the

35   synthesizer is the smallest step in frequency that can be made.

Resolution is usually a power of 10. A "lock up time" of the
synthesizer is the time it takes a new frequency to be produced
5   once a command has been made to change frequencies.

The more accurate the frequency required the longer the lock
up time. The reduction of the lock up time is a desirable goal
in synthesizer design. A modern trend is to use frequency
synthesis in wide band tuners. To tune across a wide band width
10   quickly the lock up time must be minimized. Current state of the
art tuning times for jumps in frequencies can be as short as
several microseconds. This is difficult to do when the required
increment in frequency adjustment is small. In the state of the
art indirect synthesis is capable of producing multi digit
15   resolution. However, indirect synthesis is not capable of
providing micro second switching speeds. For faster switching
speeds direct analog and direct digital technologies are used.
Therefore, it is desirable to construct an indirect frequency
synthesizer that provides high resolution and improved switching
20   speed.

The present embodiments of the invention allow all channel
selectivity and image rejection to be implemented on an
integrated circuit. Integration is a achievable by utilizing
differential signal transmission, a low phase noise oscillator,
25   integrated low Q filters, filter tuning, frequency planning,
local oscillator generation and PLL tuning to achieve a
previously unrealized level of receiver integration.

The embodiments of the invention advantageously allow a LC
filters to be integrated on a receiver chip, resulting in an
30   integrated circuit that contains substantially the entire
receiver. By advantageously selecting a frequency plan, and
utilizing the properties of complex mixers, an architecture is
achieved that allows LC filters to be integrated on a receiver
chip so that acceptable performance is produced when converting

35

a received signal to one having a lower frequency that is easily processed.

5   The embodiments utilize particular aspects of an arbitrarily defined input spectrum to first shift the received frequencies to a higher frequency in order that interference may be more easily eliminated by filtering and then shifting the spectrum to a nominal IF for processing. This first shifting process

10   advantageously shifts interfering image signals away from a center frequency of a first LC filter bank so that the LC filter bank is more effective in reducing the interfering signal strength. To further reduce the interfering signal strength, multiple LC filters that are tuned to the same frequency are

15   cascaded, further reducing the interfering signal strength.

To reduce degradation of the desired signal the exemplary embodiments of the invention utilize a complex mixing stage following an LC filter bank to reduce the image frequency interference by an additional amount that might be necessary to

20   meet a particular image rejection target (i.e., an about 60 dB to 65 dB rejection target). A complex mixer creates a signal as a result of its normal operation that cancels an image frequency interference by the remaining amount needed to achieve satisfactory performance with LC filters.

25   The ultimate goal of a receiver is to reduce the frequency of an incoming signal to a frequency that is lower than received, so that processing of the desired signal can be easily achieved. The receiver architecture utilizes two frequency down conversions to achieve this goal. Each frequency conversion is susceptible

30   to interference that requires filtering. Frequency planning as described above used in conjunction with LC filters and complex mixers, provides the required image distortion rejection that allows LC filters to be used advantageously in an integrated receiver.

35

Radio receivers require one or more local oscillator (LO) signals in order to accomplish frequency conversion to an intermediate (IF) frequency. In a typical receiver these local oscillator signals must be stable and free from noise. When a receiver is fabricated as an integrated circuit, the chances of injecting noise via the LO signals increases. Local oscillator signals for a receiver are typically generated in close proximity to the frequency conversion circuitry. The close proximity of this frequency generation circuitry to the signal path creates an increased likelihood of noise being radiated or conducted to cause interference with the received signal.

In order to achieve improved noise immunity the exemplary embodiments of the invention may utilize circuitry to generate the local oscillator signals that possess superior noise performance. The local oscillator signals may also be advantageously transmitted differentially to the mixers present on the integrated circuit. It should be noted that in alternate embodiments of the invention that a single ended output can be produced from the differential signal by various techniques known in the art. This technique is used advantageously whenever external connections to the receiver are required that are single ended.

OSCILLATOR

An exemplary embodiment of the present invention utilizes a differential oscillator having low phase noise or jitter and high isolation, as a frequency reference that substantially increases the performance of a tuner architecture integrated onto a single silicon substrate.

In accordance with the present invention, a crystal oscillator circuit is provided and constructed so as to define a periodic, sinusoidal, balanced differential signal across two symmetrical terminals of a crystal resonator which are coupled

in a parallel configuration across symmetrical, differential terminals of a differential oscillator circuit.

5   The differential oscillator circuit is configured such that it is constructed of simple active and passive components which are easily implemented in modern integrated circuit technology, thus allowing the differential oscillator circuit to be accommodated on a monolithic integrated circuit chip for which
10   the crystal oscillator (as a whole) is providing a suitable, stable periodic timing reference signal. Similarly, and in contrast to prior art implementations, only the resonating crystal (crystal resonator or quartz crystal resonator) is provided as an off-chip component. This particular configuration
15   allows for considerable savings in component parts costs by partitioning more and more functionality into the integrated circuit chip.

Remote (off chip) mounting of the crystal resonator requires that electrical contact between the crystal resonator and the
20   associated oscillator circuit, be made with interconnecting leads of finite length. In integrated circuit technology, these interconnecting leads are typically implemented as circuit pads and conductive wires formed on a PC board substrate to which package leads are bonded (soldered) in order to effect electrical
25   connection between the crystal resonator and an associated oscillator circuit. External electrical connections of this type are well known as being susceptible to noise and other forms of interference that might be radiated onto the interconnecting leads and, thence, into the oscillator circuit, degrading its
30   overall noise performance.

A sinusoidal signal source, having a differential output configuration, defines a pair of periodic sinusoidal signals, with the signal at one output terminal defined as being 180° out of phase with a similar periodic, sinusoidal signal appearing at
35   the other output terminal. Classical differential signals are

termed "balanced" in that both signals exhibit equal peek-to-peek amplitudes although they exhibit a 180° phase relationship. As illustrated in the simplified timing diagram of FIG. 6, differential signals have a particular advantage in that common-mode interference, that is injected on either terminal, is canceled when the signal is converted to single-ended. Such common mode interference is typically of equal amplitude on each pin and is caused by radiation into the circuit from external sources or is often generated in the circuit itself. In FIG. 6, a positive sinusoidal signal, denoted signal-P oscillates about a zero reference, but is shifted by a common-mode interference component, denoted I_{CM}. Likewise, a negative sinusoidal signal, denoted at signal-n, also oscillates about a zero reference, exhibiting a 180° phase relationship with signal-p, and is also offset by a common mode interference component denoted I_{CM}.

A superposition of the positive and negative periodic signals is illustrated in the timing diagram denoted "composite", which clearly illustrates that the peek-to-peek difference between the positive and negative signals remains the same, even in the presence of a common mode interference component I_{CM}.

Turning now to FIG. 7, there is depicted a semi-schematic block diagram of a periodic signal generation circuit including a differential crystal oscillator driving a differential linear buffer amplifier. Advantageously, the present invention contemplates differential signal transmission throughout its architecture to maintain the purity of the derived periodic signal and to minimize any common mode interference components injected into the system. In particular, the present invention incorporates differential signal transmission in the construction of a differential crystal oscillator circuit, including a crystal resonator and its associated oscillator driver circuit. Differential signal transmission is maintained through at least a first linear buffer stage which functions to isolate the

differential oscillator circuit switch transients and other forms
of noise that might be generated by follow-on digital integrated
5   circuit components.

In FIG. 7, a differential crystal oscillator circuit is
configured to function as a source of stable, synchronous and
periodic signals. According to the illustrated embodiment, a
differential crystal oscillator 710 suitably incorporates a
10   resonating crystal 712 and a pair of symmetrical load capacitors
714 and 716, each load capacitor respectively coupled between
ground potential and one of the two symmetrical output terminals
of the resonating crystal 712.

Resonating crystal 712 is coupled between differential
15   terminals of a differential oscillator driver circuit 718, in
turn connected to differential inputs of a differential linear
buffer integrated circuit 720. The symmetrical terminals of the
resonating crystal 712 are coupled across differential terminals
of the resonator and linear buffer, with a first terminal of the
20   crystal being shunted to ground by the first shunt capacitor 14.
The second terminal of the crystal is shunted to ground by the
second shunt capacitor 716.

The oscillator driver circuit portion of the differential
crystal oscillator 710 functions, in cooperation with the crystal
25   resonator 712, to define a pure sinusoidal and differential
signal across the crystal's symmetrical terminals. As will be
developed in greater detail below, this pure sinusoidal and
differential signal is then used by the linear buffer 720 to
develop an amplified representation of periodic signals
30   synchronized to the crystal resonant frequency. These amplified
signals are also contemplated as differential inform and are
eminently suitable for driving digital wave shaping circuitry to
define various digital pulse trains useable by various forms of
digital timing circuitry, such as phase-lock-loops (PLLs),
35   frequency tunable digital filters, direct digital frequency

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synthesizers (DDFS), and the like. In other words, the system depicted in FIG. 7 might be aptly described as a periodic

5   function generator circuit, with the crystal oscillator portion 710 providing the periodicity, and with the buffer portion 720 providing the functionality.

Before entering into a detailed discussion of the construction and operation of the differential oscillator driver

10   circuit and differential linear buffer amplifier, it will be useful to describe characteristics of a resonating crystal, such as might be contemplated for use in the context of the present invention.

FIG. 8 depicts the conventional representation of a

15   resonating crystal 712 having mirror-image and symmetrical terminals 822 and 824, upon which differential periodic signals may be developed at the crystal's resonant frequency. Resonating crystals (also termed crystal resonators) may be formed from a variety of resonating materials, but most commonly are formed

20   from a piece of quartz, precisely cut along certain of its crystalline plane surfaces, and so sized and shaped as to define a particular resonant frequency from the finished piece. Resonating crystals so formed are commonly termed "quartz crystal resonators".

25   A typical representational model of the equivalent circuit of a quartz crystal resonator 712 is illustrated in simplified, semi-schematic form in FIG. 9. A quartz crystal resonator can be modeled as a two terminal resonator, with an LCR circuit, incorporating a capacitor C_m in series with an inductor L_m and a

30   resistor R_m, coupled in parallel fashion with a capacitor C_o across the two terminals. It will be understood that the particular component values of the capacitor, inductor and resistor, forming the LCR filter portion of the circuit, define the resonant characteristics of the crystal. These design values

35   may be easily adjusted by one having skill in the art in order

to implement a resonating crystal operating at any reasonably desired frequency.

5   For example, a particular exemplary embodiment of a crystal resonator might be desired to have a resonant frequency in the range of about 10 megahertz (MHz). In such a case, the equivalent circuit of such a crystal might have a typical value of about 20 femto Farads (fF) for the capacitor C_m. The inductor

10   L_m might exhibit a typical value of about 13 milli Henreys (mH), while the resistor might have a typical value of about 50 ohms. When used in a practical oscillator design, oscillation will be achieved for values of the capacitor C_0 that are less than a design worst case value. In the exemplary embodiment, worst case

15   values of 7 pico Farads (pF) might be chosen in order to ensure a design that oscillates at the desired resonant frequency over a wide range of crystal equivalent circuit values. In a practical application, the typical range of capacitance values for C_c might be from about 3 to about 4 pF.

20   FIGS. 10 and 11 are graphical representations depicting response plots of impedance and phase with respect to frequency, respectively, of a crystal resonator circuit constructed in accordance with the equivalent circuit model of FIG. 9 and using the values given above for the component C_m, L_m, R_m, and C_0 parts.

25   FIG. 10 is a plot of the real portion of impedance, in ohms, as a function of the resonator's frequency and mega Hertz. FIG. 11 is a representational plot of the imaginary impedance component (expressed as phase), again expressed as a function of frequency in mega Hertz. From the representational plots, it can be

30   understood that an exemplary crystal resonator constructed in accordance with the above values exhibits a resonant frequency in the range of about 10 MHz. Further, simulation results on such a crystal resonator exhibit a steep rise in the real impedance versus frequency plot of FIG. 10 in the resonance

35   region about 10 MHz. A steep rise in real impedance in the

resonance region is indicative of a high quality factor, Q, typically exhibited by quartz crystal resonators.

5   An example of a quartz crystal resonator having the aforementioned characteristics and exhibiting a resonance fundamental at about 10 MHz is a Fox HC49U, quartz crystal resonator, manufactured and sold by Fox Electronics of Ft. Myers, Florida. It should be noted, however, that the specific values

10   of a quartz crystal resonator, including its resonant frequency, are not particularly important to practice of principles of the invention. Any type of crystal resonator may be used as the resonator component 712 of FIG. 7, so long as it is constructed with generally symmetrical terminals which can be driven, in a

15   manner to be described in greater detail below, by an oscillator driver circuit 718 of FIG. 7 so as to develop a differential, sinusoidal signal with respect to the two terminals. Further, the resonator need not oscillate at a frequency of 10 MHz. The choice of resonant frequency is solely a function of a circuit

20   designer's preference and necessarily depends on the frequency plan of an integrated circuit in which the system of the invention is used to provide periodic timing signals.

Turning now to FIG. 12, there is depicted a simplified schematic diagram of a differential oscillator driver circuit,

25   indicated generally at 718, suitable for differential coupling to a crystal resonator in order to develop balanced, differential sinusoidal signals for use by downstream components.

In the exemplary embodiment of FIG. 12, the differential oscillator driver circuit 718 is constructed using common

30   integrated circuit components and is symmetrical about a central axis. The oscillator driver 718 is constructed with a pair of P-channel transistors 1226 and 1228 having their source terminals coupled in common and to a current source 1230 connected, in turn, between the common source terminals and a positive supply

35   potential V_{DD}. The gate terminals of each of the P-channel

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transistors 1226 and 1228 are coupled to the drain nodes of the
opposite transistor, i.e., the gate terminal of P-channel
5   transistor 1228 is coupled to the drain node of P-channel
transistor 1226, and *vice versa*.

Output terminals are defined at each of the transistor's
drain nodes, with the drain node of P-channel transistor 1226
defining the "negative" terminal (Von) and the drain terminal of
10   P-channel transistor 1228 defining the "positive" output (Vop).
Thus, it will be understood that the circuit is able to operate
differentially by cross coupling the transistors 1226 and 1228
in order to provide feedback.

Because transistors exhibit some measure of gain at all
15   frequencies, particularly DC, conventional cross coupled
transistors are often implemented as latches in digital circuit
applications where large DC components are present. In the
differential oscillator driver circuit 718 of the invention,
latching is prevented by removing the DC gain component, while
20   retaining the system's high frequency gain, particularly gain in
the desirable 10 MHz region.

In order to substantially eliminate the gain component at
low frequencies, a high pass filter is interposed between the
gate and output terminals of each symmetrical half of the
25   circuit. In particular, a high pass filter 1232 is coupled
between the "negative" output terminal and the gate terminal of
P-channel transistor 1228. Likewise, the high pass filter 1234
is coupled between the "positive" output terminal and the gate
terminal of P-channel transistor 1226. Further, each of the high
30   pass filters 1232 and 1234 are coupled between a virtual ground,
identified as Vmid and indicated in phantom in the exemplary
embodiment of FIG. 12, and the corresponding gate terminal of the
respective one of the differential pair P-channel transistors
1226 and 1228. Each of the high pass filters 1232 and 1234 are
35   implemented as RC filters, each including a resistor and

capacitor in a series-parallel configuration. Each capacitor is
series-connected between an output terminal and the gate terminal

5   of a corresponding differential pair transistor, while each
resistor is coupled between a gate terminal and the virtual
ground. Thus, the first high pass filter 1232 includes a
capacitor 1236 coupled between the "negative" terminal and the
gate terminal of P-channel transistor 1228. A resistor 1238 is

10   coupled between the gate of P-channel transistor 1228 and virtual
ground. Similarly, the second high pass filter 1234 includes a
capacitor 1240 coupled between the "positive" terminal and the
gate terminal of P-channel transistor 1226. A resistor 1242 is
coupled between the gate of P-channel transistor 1226 and the

15   virtual ground.

In operation, high pass filter 1232 filters the input from
Von prior to applying that signal to the gate of its respective
differential pair transistor 1228. In like manner, high pass
filter 1234 filters the input from Vop prior to applying that

20   signal to the gate of its respective differential pair transistor
1226. Each of the high pass filters are symmetrically designed
and have component values chosen to give cutoff frequencies in
the range of about 5 MHz. For example, filter capacitors 1236
and 1240 might have values of about 1.5 pF, and filter resistors

25   1238 and 1242 might have values in the range of about 718 Kohms.
Which would give a filter yielding the desired 5 MHz cutoff. It
will be thus understood that the differential oscillator driver
circuit 18 will have negligible gain at DC, while exhibiting its
design gain values in the desired region of about 10 MHz.

30   It should be understood that the component values for high
pass filters 1232 and 1234 were chosen to give a particular cut
off frequency of about 5 MHz, allowing the oscillator driver
circuit to exhibit full design gain at a resonate frequency of
about 10 MHz.   If the resonant frequency of the crystal

35   oscillator circuit were required to have a different value, the

components of the high pass filters 1232 and 1234 would
necessarily take on different values to accommodate the different
5   operational characteristics of the circuit. Accordingly, the
actual component values, as well as the cutoff frequency value
of the exemplary embodiment, should not be taken as limiting the
differential oscillator driver circuit according to the invention
in any way. The values and characteristics of the differential
10 oscillator driver circuit 18 of FIG. 12 are exemplary and have
been chosen to illustrate only one particular application.

Because the common mode output signal of a differential
amplifier is often undefined, the differential oscillator driver
circuit 718 of FIG. 12 is provided with a common mode control
15 circuit which functions to maintain any common mode output signal
at reasonable levels. In particular, a differential pair of
N-channel transistors 1244 and 1246 is provided with each having
its drain terminal coupled to a respective one of the Von and Vop
output terminals. The differential N-channel transistors 1244
20 and 1246 further have their source terminals tied together in
common and to a negative supply potential V_{ss}. Their gate
terminals are tied together in common and are further coupled,
in feedback fashion, to each transistor's drain node through a
respective bias resistor 1248 and 1250. The bias resistors 1248
25 and 1250 each have a value, in the exemplary embodiment, of about
100 Kohms, with the gate terminals of the N-channel differential
pair 1244 and 1246 coupled to a center tab between the resistors.
This center tab defines the virtual ground Vmid which corresponds
to a signal midpoint about which the sinusoidal signals Von and
30 Vop oscillate. Any common mode component present at the outputs
will cause a voltage excursion to appear at the gates of the
N-channel differential pair 1244 and 1246. In other words,
virtual ground Vmid can be thought of as an operational threshold
for the current mode control differential pair 1244 and 1246.
35 Common mode excursions above or below Vmid will cause a common

mode control differential pair to adjust the circuit's operational characteristics so as to maintain Vmid at a virtual
5   ground level, thus minimizing any common mode component.

In operation, noise in such a linear differential oscillator driver circuit is filtered mainly by the crystal resonator, but also by the operational characteristics of the driver circuit. For example, noise at 10 MHz is amplified by the positive
10   feedback characteristics of the circuit and will continue to grow unless it is limited. In the exemplary embodiment of FIG. 12, signals in the 10 MHz region will continue to grow in amplitude until limited by a non-linear self-limiting gain compression mechanism.

15   As the amplitude of the amplified signal becomes large, the effective transconductance g_m of the P-channel differential pair transistors 1226 and 1228 fall off, thus limiting the gain of the differential amplifier. Amplifier gain falloff with increasing gate voltage excursions is a well understood principle, and need
20   not be described in any further detail herein. However, it should be mentioned that as the gain of the oscillator driver circuit trends to 1 the crystal resonator begins to self-limit, thus defining a constant output amplitude sinusoidal signal. Constancy of the amplitude excursions are reflected to the
25   control (gate) terminals of the P-channel differential pair 1226 and 1228 where the feedback mechanism ensures stability about unity gain.

It should be understood therefore that the differential oscillator driver circuit 718 in combination with a crystal
30   resonator (712 of FIG. 7) function to define periodic, sinusoidal and differential signals across the terminals of the crystal resonator. The signals are differential in that they maintain a 180° phase relationship. Signal quality is promoted because the exemplary differential oscillator driver circuit is designed
35   to be highly linear with a relatively low gain, thus reducing

phase noise (phase jitter) to a significantly better degree than has been achieved in the prior art. Signal quality and symmetry

5   is further enhanced by the symmetrical nature of the two halves of the oscillator driver circuit. Specifically, the oscillator driver circuit is symmetrical about a central axis and, when implemented in integrated circuit technology, that symmetry is maintained during design and layout. Thus, conductive signal

10   paths and the spatial orientation of the driver's active and passive components are identical with respect to the "negative" and "positive" outputs, thereby enhancing signal symmetry and further minimizing phase jitter.

In accordance with the invention, differential crystal

15   oscillator circuit is able to provide a periodic clock signal (approximately 10 MHz) that exhibits stable and robust timing characteristics with very low jitter. As depicted in the simplified semi-schematic block diagram of FIG. 13, a particular exemplary embodiment of a periodic signal generator circuit

20   incorporates a differential crystal oscillator circuit according to the present invention, including a crystal resonator 12 and differential oscillator driver circuit 718. A resonant crystal circuit 12 includes first and second timing capacitors (714 and 716 of FIG. 7) which are not shown merely for convenience in ease

25   of explanation. The resonant crystal circuit 712 is coupled, in parallel fashion, across the output terminals of the oscillator driver circuit 718 which incorporates the active device circuitry for pumping energy into the circuit in order to sustain oscillation. This parallel combination is coupled,

30   differentially, into a linear buffer amplifier 720, which functions to provide a linear gain factor K to the differential signal provided by the crystal oscillator circuit.

Linear buffer amplifier 720 provides signal isolation, through high input impedance, as well as amplification of the

35   oscillating (10 MHz) signal produced by the crystal

resonator/oscillator driver combination. Linear buffer amplifier
720 is configured to output differential mode signals
characterized by linear amplification of the input differential
signals, that may then be used to drive one or more additional
wave shaping-type devices, such as nonlinear buffer amplifiers
1352, 1354 and 1356.

In the exemplary embodiment of FIG. 13, the nonlinear
buffers 1352, 1354 and 1356 function in order to provide signal
translation (wave shaping) from the differential sign wave
periodic signal present at the output of the linear buffer 720
to a digital pulse train at characteristic logic levels suitable
for driving fall-on digital circuit blocks 1358, 1360 and 1362.
In addition to its signal translation function, nonlinear buffers
1352, 1354 and 1356 also provide a measure of signal
conditioning, transforming the purely sinusoidal signal at their
inputs to a very low jittergetter square wave output.

Following digital circuitry 1358, 1360 and 1362 illustrated
in the exemplary embodiment of FIG. 13 might be any type of
digital circuitry that requires a stable periodic clock, such as
a phase-lock-loop, a tunable filter, a digital frequency
synthesizer, and the like. Characteristically, high speed
switching circuits of these types generate a great deal of noise,
particularly as a result of ground bounce, switch transients and
ringing. In order to minimize feed through coupling of these
noise sources back to the crystal oscillator circuit, and in
contrast to the prior art, the system of the present invention
utilizes two stages of buffering.

In the prior art, signal transformation from a sinusoidal
signal to a square wave output is typically implemented by using
an inverter to square sinusoidal input signal. A digital
inverter function might be characterized as a nonlinear amplifier
of a transformed sinusoidal input signal to a square wave by
providing an extremely high gain, such that the input signal is

driven to the rail during amplification (i.e., clipping). Thus, the output signal of a typical inverter might be characterized

5   as a clipped sine wave. This particular nonlinearity characteristic of the inverter further provides opportunities for phase noise to be added to the output signal.

Phase noise (phase jitter) can also be introduced when the slope of a signal waveform going through a zero transition is not

10   sharp. Thus, in the present invention, phase noise is minimized in the nonlinear buffer amplifiers 1352, 1354 and 1356 by amplifying the differential signal provided by the crystal oscillator circuit through the linear amplifier 720 in order to increase the amplitude, and thus the slew rate, of the signal

15   prior to its conversion to a square wave. Phase noise resulting from zero crossings of the nonlinear buffer amplifiers is thereby minimized.

Further, in a very large scale integrated circuit, there are a great number of digital logic elements coupled to a common

20   power supply. Switching of these digital logic elements causes the power supply voltage to move up and down, causing digital switching noise. This movement in the power supply induces a jitter component at each inverter that is used as a buffer in a conventional oscillator circuit. According to the present

25   invention, maintaining a differential signal throughout the oscillator circuit, including the wave shaping buffers, allows the effects of power supply noise to be substantially eliminated from the oscillator, thus maintaining signal quality. In addition, the use of a differential signal throughout the

30   oscillator's architecture allows common mode noise radiated onto the pins of the crystal resonator to be rejected.

The number of nonlinear buffers which might be cascaded in order to produce a suitable clock signal is an additional important feature in the design of a low phase noise oscillator

35   circuit. In conventional oscillator circuits, multiple cascaded

invertors are used to provide high isolation of the final, squared output signal. In such cases, each time the signal passes through a nonlinear inverter, zero crossing occurs which offers an additional opportunity for phase noise to be added to the circuit. In order to minimize phase noise, the present invention contemplates a single stage of nonlinear buffering which presents a high input impedance to the linear buffer 720 which proceeds it. Additionally, the linear buffer 720 is further provided with a high input impedance to further isolate the crystal resonator and its associated differential oscillator driver circuitry from noise loading.

An exemplary embodiment of a linear buffer suitable for use in connection with the periodic signal generation circuit of FIG. 13 is illustrated in simplified, semi-schematic form in FIG. 14. The exemplary embodiment of FIG. 14 illustrates the conceptual implementation of a differential-in differential-out amplifier. The differential implementation has several advantages when considered in practical applications. In particular, maximum signal swing is improved by a factor of 2 because of the differential configuration. Additionally, because the signal path is balanced, signals injected due to power supply variation and switch transient noise are greatly reduced.

The exemplary implementation of a differential-in, differential-out amplifier (indicated generally at 720) of FIG. 14 uses a folded cascade configuration to produce a differential output signal, denoted V_{out}. Since the common-mode output signal of amplifiers having a differential output can often be indeterminate, and thus cause the amplifier to drift from the region where high gain is achieved, it is desirable to provide some form of common-mode feedback in order to stabilize the common-mode output signal. In the embodiment of FIG. 14, the common-mode output signal is sampled, at each of the terminals

comprising the output V_{out} and fed back to the current-sink loads of the folded cascade.

5   Differential input signals V_{in} are provided to the control terminals of a differential input pair 1464 and 1466, themselves coupled between respective current sources 1468 and 1470 and to a common current-sink load 1472 to V_{ss}. Two additional transistors (P-channel transistors in the exemplary embodiment

10   of FIG. 14) define the cascade elements for current-sources 1468 and 1470 and provide bias current to the amplifier circuit.

High impedance current-sink loads at the output of the amplifier 1476 and 1478 might be implemented by cascoded current sink transistors (N-channel transistors for example) resulting

15   in an output impedance in the region of about 1 Mohm. The common mode feedback circuit 1480 might be implemented as an N-channel differential pair, biased in their active regions and which sample the common-mode output signal and feedback a correcting, common-mode signal into the source terminals of the cascoded

20   transistors forming the current-sinks 1476 and 1478. The cascade devices amplify this compensating signal in order to restore the common-mode output voltage to its original level.

It should be noted that the exemplary linear amplifier of FIG. 14 might be implemented as any one of a number of

25   appropriate alternative amplifiers. For example, it need not be implemented as a fully differential folded cascade amplifier, but might rather be implemented as a differential-in, differential-out op amp using two differential-in single-ended out op amps. Further, the actual circuit implementation might certainly vary

30   depending on the particular choices and prejudices of an analog integrated circuit designer. The input differential pair might be either an N-channel or a P-channel pair, MOS devices might be used differentially as active resistors or alternatively, passive resistor components might be provided, and the like. All that

35   is required is that the linear amplifier 720 amplifies a

differential input signal to produce a differential, sinusoidal signal at its output. Thus, the only frequency components

5   reflected back through the linear amplifier 720 will be sinusoidal in nature and thus, will not affect the operational parameters of the differential crystal oscillator frequency. Further, the linear buffer 720 will necessarily have a relatively high output impedance in order to attenuate noise that might be

10   reflected back from the square wave output of the following nonlinear amplifier stages.

Turning now to FIG. 15, there is depicted a simplified semi-schematic diagram of a nonlinear buffer, indicated generally at 1582, such as might be implemented as a wave shaping or

15   squaring circuit 1352, 1354 or 1356 of FIG. 13. The nonlinear buffer 1582 receives a differential, sinusoidal input signal at the gate terminals of an input differential transistor pair 1584 and 1586. Drain terminals of the differential pair 1584 and 1586 are connected together in common and to a current sink supply

20   1588 which is coupled to a negative potential. Each of the differential pairs' respective source terminals are coupled to a bias network, including a pair of differential bias transistors 1590 and 1592 having their gate terminals tied together in common and coupled to a parallel connected bias network. The bias

25   network is suitably constructed of a resistor 1594 and a current sink 1596 connected in series between a positive voltage potential such as Vdd and Vss. A bias node between the resistor 1594 and current sink 1596 is coupled to the common gate terminals of the bias transistor network 1590 and 1592 and

30   defines a bias voltage for the bias network which will be understood to be the positive supply value minus the IR drop across bias resistor 1594. The current promoting the IR drop across the bias resistor 1594 is, necessarily, the current I developed by the current sink 1596.

35

A differential, square wave-type output (Vout) is developed at two output nodes disposed between the respective source
5   terminals of the bias network transistors 1590 and 1592 and a respective pair of pull-up resistors 1598 and 1599 coupled, in turn, to the positive supply potential. It should be noted, that the bias network, including transistors 1590 and 1592, function to control the non-linear amplifier's common mode response in a
10   manner similar to the linear amplifier's common mode network (transistors 1244 and 1246 and resistors 1248 and 1250 of FIG. 12).

Although depicted and constructed so as to generate a differential square wave-type output in response to a
15   differential sinusoidal input signal, the non-linear buffer 1582 of FIG. 15 is well suited for single-ended applications as well as for differential applications. If a single-ended output is desired, one need only take a signal from one of the two symmetric outputs. The choice of whether to implement the
20   non-linear buffer as a single-ended or a differential buffer will depend solely on the input requirements of any follow-on digital circuitry which the periodic signal generation circuit in accordance with the invention is intended to clock. This option is solely at the discretion of the system designer and has no
25   particular bearing on practice of principles of the invention.

FIG. 16 is a semi-schematic illustration of an alternative embodiment of the differential oscillator driver circuit (718 of FIG. 12). From the exemplary embodiment of FIG. 16, it can be understood that the oscillator driver circuit is constructed in
30   a manner substantially similar to the exemplary embodiment of FIG. 12, except that a crystal resonator is coupled across the circuit halves above the differential transistor pair, as opposed to being coupled across a circuit from the Von to Vop output terminals. The alternative configuration of FIG. 16 operates in
35   substantially the same manner as the embodiment of FIG. 12 and

produces the same benefits as the earlier disclosed oscillator.
It is offered here as an alternative embodiment only for purposes
5   of completeness and to illustrate that the specific arrangement
of the embodiment of FIG. 12 need not be followed with slavish
precision.

It should be understood that oscillator circuits with low
phase noise are highly desirable in many particular applications.
10 FIG. 17 illustrates one such application as a reference signal
generator in a phase-lock-loop. The phase-lock-loop uses a low
phase noise periodic signal generation circuit in accordance with
the invention in order to generate a reference signal for use by
a phase detector. Providing a clean reference signal to the
15 phase detector is fundamental to providing a clean RF output from
the PLL. Since noise and nonlinearities induced by signal
generation circuit are carried through the PLL circuit, thus
degrading the RF output, reducing phase noise and providing noise
rejection early on in the signal processing chain is advantageous
20 to maintaining a clean RF output. A differential crystal
oscillator (710 of FIG. 7) advantageously provides this claim
signal by maintaining a differential signal across the terminals
of the resonating crystal, an improvement not currently available
in state-of-the-art crystal oscillators. Additionally, the use
25 of linear buffer amplifiers followed by nonlinear amplification
in a reference oscillator circuit is a unique improvement over
the prior art in reducing phase noise.

Since PLLs have become available in integrated circuit form,
they have been found to be useful in many applications. Certain
30 examples of advantageous application of phase-lock-loop
technology include tracking filters, FSK decoders, FM stereo
decoders, FM demodulators, frequency synthesizers and frequency
multipliers and dividers. PLLs are used extensively for the
generation of local oscillator frequencies in TV and radio
35 tuners. The attractiveness of the PLL lies in the fact that it

may be used to generate signals which are phase-locked to a
crystal reference and which exhibit the same stability as the
5   crystal reference. In addition, a PLL is able to act as a narrow
band filter, i.e., tracking a signal whose frequency may be
varying.

A PLL uses a frequency reference source in the control loop
in order to control the frequency and phase of a voltage control
10   oscillator (VCO) in the loop. The VCO frequency may be the same
as the reference frequency or may be a multiple of the reference
frequency. With a programmable divider inserted into the loop,
a VCO is able to generate a multiple of the input frequency with
a precise phase relationship between a reference frequency and
15   an RF output. In order to maintain such a precise phase and
frequency relationship, the frequency reference provided to the
PLL must, necessarily, also be precise and stable.

FIG. 18 is a simplified block diagram of an illustrative
frequency synthesizer that might incorporate the differential
20   periodic signal generation circuit of the invention. The
frequency synthesizer is a signal generator that can be switched
to output any one of a discrete set of frequencies and whose
frequency stability is derived from a crystal oscillator circuit.

Frequency synthesizers might be chosen over other forms of
25   frequency sources when the design goal is to produce a pure
frequency that is relatively free of spurious outputs.
Particular design goals in frequency synthesizer design might
include suppression of unwanted frequencies and the suppression
of noise in a region close to the resonant frequency of the
30   crystal that is a typical source of unwanted phase modulation.
Synonymous terms for this type of noise are broadband phase
noise, spectral density distribution of phase noise, residual FM,
and short term fractional frequency deviation.

To reduce the noise produced in a synthesizer, crystal
35   oscillators are commonly used due to their stability and low

noise output. The use of a periodic signal generation circuit incorporating a differential crystal oscillator according to an

5   embodiment of the present invention advantageously improves these performance parameters. Improved phase noise is achieved through the use of linear buffering followed by nonlinear amplification, while noise rejection is provided by the differential design utilized throughout the circuitry architecture.

10   It should be evident that a periodic signal generation circuit according to the invention has many uses in modern, state-of-the-art timing circuits and systems. The periodic signal generation circuit is constructed of simple active and passive components which are easily implemented in modern

15   integrated circuit technology. Thus allowing substantially all of the components to be accommodated on one monolithic integrated circuit chip for which the crystal oscillator portion is providing a suitable, stable periodic timing reference signal. Only the resonating crystal portion (crystal resonator or quartz

20   crystal resonator) is provided as an off-chip component. This particular configuration allows for considerable savings in component parts costs by partitioning more and more functionality into the integrated circuit chip itself.

A more detailed description of the oscillator is provided

25   in U.S. Patent Application No. 09/438,689 filed November 12, 1999 (B600:33758) entitled "Differential Crystal Oscillator" by Christopher M. Ward and Pieter Vorenkamp; based on U.S. Provisional Application No. 60/108,209 filed November 12, 1998 (B600:33588), the subject matter of which is incorporated in its

30   entirety by reference. The oscillator's output is a differential signal that exhibits high common mode noise rejection. Use of a low noise reference oscillator with differential signal transmission allows the synthesis of stable low noise local oscillator signals. Advantageously in the present exemplary

35   embodiment of the invention a unique generation of the local

oscillator signals allows complete integration of a receiver circuit on a CMOS integrated circuit by reducing noise in the

5   signal path.

Frequency synthesizers and a radio frequency receiver often incorporate phase locked loops that make use of a crystal oscillator as a frequency reference. A PLL is used to provide coarse tuning within the frequency band of interest while a

10   second PLL provides fine tuning steps. Advantageously, the present embodiments of the invention utilize a method of coarse/fine PLL adjustment to improve the performance of the integrated tuner.

15   COARSE/FINE PLL ADJUSTMENT

FIG. 19 is a diagram illustrating receiver tuning. The combination of a wide band PLL 1908 and a narrow band PLL 1910 tuning provides a capability to fine tune a receiver's LOS 1902, 1904 over a large bandwidth in small frequency steps. For

20   the exemplary embodiments of QAM modulation a small frequency step is 100 kHz, and 25 kHz for NTSC modulation. Fine tuning is available over an entire exemplary 50 MHz to 860 MHz impact frequency band width 1906. The first PLL 1908 tunes a first LO 1902 in large 10 MHz frequency steps and the second PLL 1910

25   tunes a second LO 1904 in much smaller steps.   The first intermediate frequency (IF) filter 1912 has a sufficiently wide band width to allow up to 10 MHz frequency error in tuning the first intermediate frequency, with the narrow band PLL providing final fine frequency tuning to achieve the desired final IF

30   frequency 1914.

FIG. 20 is a block diagram of an exemplary tuner 2002 designed to receive a 50 to 860 MHz bandwidth signal 2004 containing a multiplicity of channels. In this exemplary band of frequencies, there are 136 channels with a spacing between

35   channel center frequencies of six megahertz 2008. The tuner

selects one of these 136 channels 2006 that are at a frequency
between 50 and 860 MHz by tuning to the center frequency of the
selected channel 2010. Once a channel is selected the receiver
rejects the other channels and distortion presented to it. The
selected channel is down converted to produce a channel centered
about a 44 MHz intermediate frequency (IF) 2012. Alternatively
the value of the intermediate frequency ultimately produced by
the tuner may be selected utilizing the method of the invention
to provide any suitable final IF frequency, such as 36 MHz.

In selecting one of these 136 channels, a maximum frequency
error in the local oscillator (LO) frequency used to tune the
channel to a given IF of plus or minus 50 kHz is allowable.
Using one frequency conversion to directly tune any one of the
136 channels to 44 MHz would require a tuning range in the local
oscillator of 810 MHz. This would require a local oscillator
that tunes from 94 to 854 MHz, if utilizing high side conversion.

Achieving this with a single LO is impractical. Tuning range
in local oscillators is provided by varactor diodes that
typically require 33 volts to tune them across their tuning
range. Additionally, within this tuning range a frequency tuning
step of 100 kHz is required to ensure that the center frequency
of a tuned channel is tuned within plus or minus 50 kHz. Thus,
a large range of frequencies would have to be tuned in small
increments over a 33 volt tuning signal range.

Returning to FIG. 19 illustrating the frequency tuning
method of the invention an exemplary 50 to 860 MHz signal 1906
is presented to a first mixer 1916 that is tuned with a wide band
PLL 1908 that tunes a first LO 1902 in frequency steps of 10 MHz.
This local oscillator 1902 is set to a frequency that will
nominally center a channels that has been selected at a first IF
of 1,200 MHz 1918. The first IF 1918 is then mixed 1920 to the
second IF of 275 MHz 1922. This is done by the narrow band PLL
1910 that tunes a second LO 1904 in frequency steps of 100 kHz.

The second IF 1922 is next mixed 1924 down to a third IF 1926 of 44 MHz by a third local oscillator signal 1928. This third local

5   oscillator signal 1930 is derived from the second local oscillator or narrow band PLL signal by dividing its frequency by a factor of four.

FIG. 21 is an exemplary table of frequencies utilizing coarse and fine PLL tuning to derive a 44 MHz IF ("IF-3").

10   A process is utilized to determine the wide and narrow band PLL frequencies. The relationship between the wideband PLL and narrowband PLL frequencies to yield the desired intermediate frequency is found from:

15       $$FLO1 - Fsig - (5/4 * FLO2) = Fif \qquad\qquad (4)$$

where:

FLO1:   PLL1 frequency (10MHz steps)

FLO2:   PLL2 frequency

20   (e.g., 25kHz/100kHz/200kHz or 400kHz step)

Fsig: Input signal

Fif (e.g., 44MHz or 36MHz or whatever IF is required)

Example:

25       $1250M - 50M - (5/4 * 924.8M) = 44M$

where: Fsig = 50MHz

FLO1 = 1250MHz

FLO2 = 924.8MHz

Fif = 44MHz

30

FIG 21 and 22 utilized this formula to derive the values entered into them to tune the exemplary cable TV signals "Frf". For example the first column 2102 of the table lists the frequencies needed to tune a signal centered at 50 MHz ("Frf")

35   to a 44 MHz final IF ("IF-3").   To tune a received channel

centered at 50 MHz a first LO of 1,250 MHz ("LO-1") is provided by a wide band, or coarse, PLL. This produces a first IF of 5   1,200 MHz ("IF-1").   Next utilizing 100 kHz tuning steps to adjust LO 2, it is set to 924.8 MHz ("LO-2"). Note this is not exactly 925 MHz. Dividing the second LO by 4 in this instance yields 231.2 MHz for a third LO ("LO-3"). When LO 3 is applied to the second IF of 275.2 a third IF of 44 MHz ("IF-3") is 10   produced. This tuning arrangement is illustrated for received channels having a six MHz channel spacing as can be seen from the line entitled "Frf".   In each case the coarse fine tuning approach yields a third IF ("IF-3") of 44 MHz.

FIG. 22 is an illustration of an alternative embodiment of 15   the coarse and fine PLL tuning method to produce an exemplary final IF of 36 MHz. In this case as previously, a first IF (IF-1) is tuned to 1,200 MHz plus or minus 4 MHz. And second LO (LO-2) is close to 930 MHz, utilizing a small offset to yield a third IF of 36 MHz (IF-3). These predetermined tuning 20   frequencies are stored in a memory and applied when a command is given to tune a given channel. Alternatively an algorithm may be supplied to produce the tuning frequencies. It is understood that these frequencies are exemplary and other frequencies that utilize this method are possible.

25   Thus, it can be seen that the interaction of course and fine PLL frequencies are utilized to produce a third IF of 44 MHz. A second LO (LO-2) is maintained close to a frequency of 925 MHz to tune each of the channels. However, it is slightly off by a very small tuning step of 100 kHz. Note that the first IF (IF-1) 30   is not always right at 1,200 MHz. Sometime it is off by as much as 4 MHz either above or below 1,200 MHz. This error will still result in signal transmission through a first IF filter. The maximum error utilizing this scheme is plus or minus 4 MHz.

This method of PLL adjustment is described in more detail 35   in U.S. Patent Application No. 09/438,688 filed November 12,

1999, (B600:34015) entitled "System and Method for Coarse/Fine
PLL Adjustments" by Pieter Vorenkamp, Klaas Bult and Frank Carr;

5   based on U.S. Provisional Application No. 60/108,459 filed
November 12, 1998 (B600:33586), the subject matter of which is
incorporated in its entirety by reference.

A coarse, and a fine PLL use a common reference frequency
oscillator. Local oscillator signals produced by the frequency

10   synthesizer's phase locked loops inject noise produced in the
reference frequency oscillator and the PLLs into a signal path
through the PLL output. Noise injected can be characterized as
either phase noise or jitter. Phase noise is the frequency
domain representation of noise that, in the time domain is

15   characterized as jitter. Phase noise is typically specified as
a power level below the carrier per Hertz at a given frequency
away from the carrier. Phase noise can be mathematically
transformed to approximate a jitter at a given frequency for a
time domain signal. In a clock signal jitter refers to the

20   uncertainty in the time length between zero crossings of the
clock signal. It is desirable to minimize the jitter produced
in an oscillator circuit and transmitted through the signal chain
into the signal path to prevent noise degradation in the receiver
path. Equivalently, any oscillator producing a stable output

25   frequency will suffice to produce a reference frequency for the
PLL circuitry.

Another obstacle to integrating an entire receiver on a
single CMOS chip has been the inability to fabricate a
satisfactory filter structure on the chip. As previously

30   described, a multitude of unwanted frequencies created through
circuit non linearities are a major obstacle in achieving
satisfactory receiver performance. Filtering is one method of
eliminating these unwanted spurious signals. An integrated
filter's center frequency tends to drift, and needs calibration

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to maintain performance. To successfully use filtering on chip, an auto calibration loop is needed to center the filter response.

5   FIG. 23 is a block diagram of a dummy component used to model an operative component on an integrated circuit chips. According to one aspect of the invention, a dummy circuit on an integrated circuit chip is used to model an operative circuit that lies in a main, e.g. RF, signal path on the chip.

10   Adjustments are made to the dummy circuit in a control signal path outside the main signal path. Once the dummy circuit has been adjusted, its state is transferred to the operative circuit in the main signal path. Specifically, as shown in FIG. 23, there is a main signal path 2201 and a control signal path 2202

15   on an integrated circuit chip. In main signal path 2201, a signal source 2203 is coupled by an operative circuit 2204 to be adjusted to a load 2205. Main signal path 2201 carries RF signals. Signal source 2203 generally represents the portion of the integrated circuit chip upstream of operative circuit 2204

20   and load 2205 generally represents the portion of the integrated circuit chip downstream of operative circuit 2204. In control signal path 2202, a control circuit 2206 is connected to a dummy circuit 2207 and to operative circuit 2204. Dummy circuit 2207 is connected to control circuit 2206 to establish a feedback

25   loop. Dummy circuit 2207 replicates operative circuit 2204 in the main signal path in the sense that, having been formed in the same integrated circuit process as operative circuit 2204, its parameters, e.g., capacitance, inductance, resistance, are equal to or related to the parameters of operative circuit 2204.

30   To adjust operative circuit 2204, a signal is applied by control circuit 2206 to dummy circuit 2207. The feedback loop formed by control circuit 2206 and dummy circuit 2207 adjusts dummy circuit 2207 until it meets a prescribed criterion. By means of the open loop connection between control circuit 2206 and operative

35   circuit 2204 the state of dummy circuit 2207 is also transferred

to operative circuit 2204, either on a one-to-one or a scaled basis. Thus, operative circuit 2204 is indirectly adjusted to

5   satisfy the prescribed criterion, without having to be switched out of the main signal path and without causing disruptions or perturbations in the main signal path.

In one implementation of this dummy circuit technique described below in connection with FIGS. 24a-c and FIGS. 25-27,

10   operative circuit 2204 to be adjusted is a bank of capacitors in one or more operative bandpass filters in an RF signal path, dummy circuit 2207 is a bank of related capacitors in a dummy bandpass filter, and control circuit 2206 is a phase detector and an on-chip local oscillator to which the operative filter is to

15   be tuned. The output of the local oscillator is coupled to the dummy filter. The output of the dummy filter and the output of the local oscillator are coupled to the inputs of the phase detector to sense the difference between the frequency of the local oscillator and the frequency to which the dummy filter is

20   tuned. The output of the phase detector is coupled to the dummy filter to adjust its bank of capacitors so as to tune the dummy filter to the local oscillator frequency. After the dummy filter is tuned, the state of its capacitor bank is transferred, either on a one-to-one or scaled basis, to the operative filter. Since

25   the capacitor bank in the dummy filter replicates that of the operative filter, the frequency to which the operative filter is tuned can be easily scaled to the frequency of the dummy filter.

In another implementation of the dummy circuit technique described below in connection with FIGS. 28 to 33, operative

30   circuit 2204 to be adjusted is a filter having a spiral inductor that has a temperature sensitive internal resistance. Dummy circuit 2207 has an identical spiral inductor. Control circuit 2206 has a controllable variable resistor in series with the inductor of dummy circuit 2207. The controllable resistor is

35   driven by a feedback loop to offset changes in the internal

resistance of the inductor of dummy circuit 2207. Operative
circuit 2204 has a similar controlled resistor in series with its
5   inductor to transfer the resistance value of the controllable
resistor in control circuit 2206 to the resistor of the operative
circuit 2204 in open loop fashion.

FILTER TUNING

10   FIG. 24a is a block diagram illustrating the use of a tuning
circuit outside of a signal path to tune bandpass filters present
in a receiver. A tuning circuit 2302 utilizes a substitute or
"dummy" filter stage 2310 to derive tuning parameters for a
filter bank 2304 present in a signal path 2306. The tuning
15   circuit utilizes a local oscillator signal 2308 available in the
receiver to tune the dummy filter 2310 to the center frequency
of the local oscillator. Once tuned, the dummy filters 2310 tuned
component values that result in a tuned response at the local
oscillator frequency are scaled in frequency and applied to the
20   bandpass filter 2312. The filters are tuned at startup, and the
tuning circuitry is turned off during normal operation. This
prevents the injection of additional noise into the signal path
during operation.
         FIG. 24b is a flow diagram of the tuning process in
25   operation receiver is initially powered up 2312 and local
oscillator signals generated by PLLs are centered at their design
frequency 2314. Once the PLLs are locked their frequency is a
known condition. Next substitute filter tuning is initiated 2316
and performed. When finished a signal is received back from the
30   filter tuning network indicating that it is ready 2318.
Information from the tuning network is copied to the receive path
filter circuit 2320. Next the filter tuning circuit is turned off
2322 disconnecting it from the filter circuit. In the embodiments
of the invention the narrow band PLL (2308, of FIG. 24a) is used
35   as reference frequency in the tuning circuit. However, it is

understood that this tuning technique may be utilized with any
readily available signal.

5   Returning to FIG. 24a, in an exemplary embodiment of the
invention a 925 MHz signal is directly available from the narrow
band PLL 2308. It is used to tune the dummy filter 2310 contained
in the tuning circuit 2302 associated with the 1,200 MHz filter
2304. After the dummy filter is tuned to 925 MHz, frequency
10   scaling is used to obtain the proper component values for the
1,200 MHz filter response to be centered. The exemplary 925 MHz
signal generated by the narrow band PLL is divided by 4 to yield
a 231 MHz third LO signal utilized in additional tuning
circuitry.

15   Other divisions or multiplications may be equivalently used
to tune dummy filters. A second exemplary filter tuning circuit
2302 for a 275 MHz filter contains a dummy filter 2310 that is
tuned to a center frequency of 231 MHz.   Once tuned, the
component values used to center the 231 MHz dummy filter 2310 are
20   scaled to yield a centered response for the 275 MHz filter 2304.
At this point in time the tuning circuits 2302 are switched off.
It is especially important to turn off the exemplary tuning
circuits on the 275 MHz filter since the 231 MHz signal used to
tune its dummy filter falls in an exemplary 50-860 MHz band.

25   It is to be understood that any available frequency may be
used to tune a substitute filter so that another filter, that
does not have an appropriate tuning signal present, may be tuned.
This is done by scaling the component values of the tuned dummy
filter to values appropriate for the filter not having the tuning
30   frequency present. Tuning values obtained for a dummy filter may
be applied to all filters present in a bank of filters having a
common center frequency. Also tuning values obtained for a dummy
filter may be applied to multiple filters present having
differing center frequencies by applying differing scaling
35   factors. Finally multiple filters at different locations in a

signal path that have common center frequencies may be tuned by a common tuning circuit.

5   Capacitors disposed on an integrated circuit vary in capacitance value by as much as +/- 20%. Thus, to provide a satisfactory receiver performance a method of tuning integrated filters that removes this variation in capacitance is needed. In an LC filter circuit either an inductance or a capacitance can

10   be tuned. However, inductors are difficult to tune. Therefore, in the embodiments of the invention values of capacitance present in the filters are tuned. In tuning the exemplary embodiments, one or more capacitors are switched in and out of an LC filter circuit to tune it.

15   These capacitors are switched in and out of a filter circuit electronically. Capacitors with the same dimensions are provided in a bandpass filter and a dummy filter to provide satisfactory matching between the devices. Switchable caps in the embodiments of the invention are MOS caps that are all of the same value and

20   from factor. However, it is to be recognized that other weighting of capacitor values could be provided to achieve an equivalent function. For example, binary or 1/x weighted values of capacitors could be disposed in each filter to provide tuning. In the embodiments of the invention a bank of fixed capacitors

25   and a bank of electronically tunable capacitors are provided. The adjustable capacitors in the exemplary embodiment represent 40% of the total capacitance provided. This is done to provide for the ±20% variance in center frequency due to manufacturing variances.   To accommodate other ranges of manufacturing

30   variations or alternative tuning schemes any fraction or all of the capacitors may be switchable. It is also understood that any type of switchable capacitor, in addition to a MOS capacitor type may be utilized.

        FIGS. 24a-24c are exemplary illustrations of a tuning
35   process utilizing switched capacitors. Filter responses shown at

the bottom plot 2402 illustrate a tuning of a dummy filter 2310 that is contained in a tuning circuit 2302 of FIG. 24a. A

5   frequency response being tuned in the upper graph 2404 shows the tuning of the exemplary 1,200 MHz bandpass filter 2304 of FIG. 24a. Initially none of the switched capacitors are applied in a dummy filter circuit. This places the filter response initially 2406 above the final desired tuned response frequency

10   2408.   In this example capacitors are added until the filter response of the dummy filter is centered about 925 MHz. However, the tuned response of the 925 MHz dummy filter 2408 is not the desired center frequency of the bandpass filter in the signal path. The values used in to tune the dummy filter would not tune

15   the 1,200 MHz filter to the correct response. Frequency scaling is used to tune the desired response. This can be achieved because identical capacitors disposed on a chip are very well matched in value and parasitics. In particular capacitor matching is easy to achieve by maintaining similar dimensions between

20   groups of capacitors. In scaling a response to determine a capacitance to apply in a bandpass filter, identical inductance values have been maintained in the dummy and bandpass circuits. Thus, only a scaling of the capacitors is necessary. The frequency relation in the exemplary embodiment is given by the

25   ratio:

$$\frac{1}{2} \approx \sqrt{\frac{(L_2)(C_2)}{(L_1)(C_1)}} \tag{5}$$

For this particular embodiment utilizing identical inductor

30   values $L_1 = L_2$. This reduces to:

$$\frac{f_1}{f_2} \approx \sqrt{\frac{(C_2)}{(C_1)}} \tag{6}$$

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For the exemplary embodiment this is equal to 925/1200, or a capacitance ratio of 3:5. However, it is understood that other
5   ratios will allow tuning to be performed equivalently.

Returning to FIG. 24a various control signals applied to the tuning circuit are shown. In the event that the tuning is slightly off after the tuning procedure, an offset control circuit is provided within the tuning circuit of FIG. 24a to move
10   the tuning of the filters up or down slightly by providing a manual means of adding or removing a capacitor. This control is shown by an "up/down" control line 2324 of FIG. 24a. The exemplary tuning circuit of FIG. 24a is additionally provided with a "LO" 2308 tuning frequency to tune the dummy filter. The
15   "10 MHz reference" signal 2326 is utilized as a clock in the tuning circuit that controls the sequence of adding capacitors. The "reset" signal 2328 resets the tuning circuit for the next tuning cycle.

FIG. 25 is a block diagram of an exemplary tuning circuit.
20   A reset signal 2502 is utilized to eliminate all the capacitors from the circuit at power up by resetting a counter 2504 that controls the application of the switched capacitors. The reset signal may be initiated by a controller or generated locally. This provides a known starting point for filter tuning. Next a
25   filter figure of merit is examined to determine iteratively when to stop tuning.

FIG. 26 illustrates the amplitude 2602 and phase 2604 relationship in an LC filter tuned to its center frequency, fc. In tuning a filter to a center frequency two responses are
30   available for examination. Amplitude and phase response are parameters that may be used to tune the filter. For a wide band LC filter amplitude response 2602 is not the optimal parameter to monitor. At the center frequency the top of the response curve is flat making it difficult to judge if the response is exactly
35   centered. The phase response 2604 however, has a rather

pronounced slope at the center frequency. The steep slope of the
phase signal provides an easily discernable transition for
5   determining when the center frequency has been reached.

Returning to FIG. 25, phase detection is used to detect when
a dummy filter 2506 has been tuned. An exemplary 925 MHz input
from a narrow band PLL is input 2508 to a phase detector 2510.
The phase detector compares the phase of a signal input to a
10   dummy filter 2508 to a phase of the output 2512 of that filter
2506. The phase detector produces a signal that is internally low
pass filtered to produce a DC signal 2514 proportional to the
phase difference of the two input signals 2512, 2508. When tuned
there is a 90 degree phase shift across capacitors internal to
15   the phase detector, that corresponds to 0 degrees of phase shift
across the filter. Zero (0) degrees of phase shift produces a
0 volt output. Since it is known that with the capacitors
switched out of the filter circuit 2506 that the center frequency
of the filter is high, the comparator 2516 following the low pass
20   filter is designed to output 2518 a high signal that enables
filter capacitors to be switched in until the phase detector 2510
indicates no phase difference is present across the filter 2506
at the tuned frequency. With a zero degree phase shift detected
the comparator 2516 disables the counter preventing any further
25   capacitors from being switched into the filter circuit.

The phase detector 2510 of the exemplary embodiment utilizes
a gilbert cell mixer 2512 and an integral low pan filter 2525 to
detect phase. However, other phase detectors may be equivalently
substituted for the mixer circuit. The 90° phase shift between
30   an i port 2508 and a q port 2512 is being detected by the mixer.
A 90° phase shift between the i and the q signals in the mixer
provides a 0 volt output indicating that those signals are in
quadrature relation to each other. The signals are shown as
differential signals, however single ended signals may
35   equivalently be used.

The phase detector out 2514 is next fed into a comparator 2516 that is set to trip on a zero crossing detected at its

5   input. When a zero crossing is encountered as the phase detector output approaches zero, the comparator latches and a counter 2504 is shut off and reset 2518. The comparator function is equivalently provided by any standard comparator circuit known by those skilled in the art.

10   The counter 2504 counts based on the 10 MHz reference clock 2524, although many periodic signals will suffice as a clock. As the counter advances more filter capacitors are switched into the circuit. In the embodiments of the invention 15 control lines 2526 are used to simultaneously switch the capacitors into the

15   dummy filter and the bandpass filter bank. The control lines remain hard wired to both filters 2528, 2506, and are not switched off. However, once the comparator 2516 shuts the counter 2504 off the tuning circuit 2530 is inactive and does not affect the band pass filter 2520 in the signal path.

20   FIG. 27 is a schematic diagram showing the internal configuration of switchable capacitors in a differential signal transmission embodiment of the dummy filter 2506 and the construction of the phase detector 2510. A set of fifteen control lines 2526 are utilized to switch fifteen pair of MOS

25   capacitors 2702 on and off. The capacitors are switched in and out by applying a given control signal to a virtual ground point 2704 in this configuration. Thus, when the capacitors are connected as shown the control signal is being applied at a virtual ground. Thus, parasitic capacitances at this point will

30   not affect the filter 2506 performance. A gain producing LC stage 2706 of the dummy filter is of a differential configuration and has its LC elements 2708 connected in parallel with the MOS capacitors 2702.

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Thus, with a capacitance ratio of 3:5 being utilized in the exemplary one line of embodiment a hard wired bus 2526 going to
5   the dummy filter 2506 will switch in 5 unit capacitors, while the other end of the line that goes to the bandpass filter (2528 of FIG. 25) in the signal path will switch in 3 unit capacitors.

In the mixer circuit that is used as a phase detector 2710 in the exemplary embodiment, differential image ("i") signals I_P
10   and I_N and differential quadrature ("q") signals Q_P and Q_N are input to the phase detector. A conventional Gilbert cell mixer configured as a phase detector 2710, as shown, has delay between the i port 2508 and q port 2512 to the output 2514. The i delay to the output tends to be longer due to the fact that it must
15   travel through a greater number of transistors than the q input to output path. Thus, even if i and q are exactly 90 degrees out of phase a DC offset tends to produced due to the path length differences causing a phase error. To remedy this situation a second Gilbert cell mixer is duplicated 2710 and connected in
20   parallel with the first 2710. However, the i port and the q port connected to the mixer 2712 are swapped to average out the delay thus tending to reduce the offset. This results in an almost 0° output phase error that is independent of frequency. Other types of phase detectors and other means of equalizing the delay, such
25   as a delay line are understood by those skilled in the art to provide an equivalent function.

In the embodiment shown, the loss pass filter is implemented by a single capacitor 2714 at each output. However, other equivalent methods of achieving a low pass filter known to those
30   skilled in the art are acceptable as well.

A method of filter tuning the advantageously uses the frequency synthesizer output is fully described in U.S. Patent Application No. 09/438,234 filed November 12, 1999 (B600:34013) entitled "System and Method for On-Chip Filter Tuning" by Pieter
35   Vorenkamp, Klaas Bult and Frank Carr; based on U.S. Provisional

1   36664/PBH/B600 (BP 1298)

Application No. 60/108,459 filed November 12, 1998 (B600:33586),
the subject matter of which is incorporated in its entirety by
5   reference.

          Filters contain circuit elements whose values are frequency
and temperature dependent. The lower the frequency, the larger
the size of the element required to realize a given value. These
frequency dependent circuit elements are capacitors and
10   inductors. The fabrication of capacitors is not as problematic
as the fabrication of inductors on an integrated circuit.
Inductors require relatively more space, and because of their
size has a temperature dependent Q.

15   ACTIVE FILTER MULTI-TRACK INTEGRATED SPIRAL INDUCTOR
          FIG. 28a is a plan view of a multi-track spiral inductor
2800 suitable for integration onto an integrated circuit, such
as one produced with a CMOS process. A standard CMOS process
often utilizes a limited number of layers and a doped substrate.
20   These conditions do not provide optimum conditions for
fabrication an on chip inductor. Currents induced in the heavily
doped substrate tend to be a source of significant losses. The
multi-track inductor 2800 is made from several long narrow strips
of metal 2804, 2806 connected in parallel 2808, 2810 and disposed
25   upon an integrated circuit substrate 2802.   A multi-track
integrated spiral inductor tends to produce an inductance with
a higher Q. High Q is desirable to achieve lower noise floors,
lower phase noise in oscillators and when used in filters, a
better selectivity.   To reduce series resistance and thus
30   improves the Q of a spiral inductor, a single wide track width
in the spiral is typically used by those skilled in the art.
          Skin effect is a frequency dependent phenomena, occurring
where a given current is present in a conductor, that produces
a current density in the conductor. At DC, where the frequency
35   is zero, the current density is evenly distributed across a

conductor's cross section. As the frequency is increased the current crowds to the surface of the conductor. At high

5   frequency substantially all of the current tends to flow in the surface of the conductor. Thus, the current density at the center of the conductor is very low, and at the surface it is greater. A skin depth is the depth in the conductor (δ) at which the current is $1/e=0.368$ the value of the current on the surface.

10   The equation for skin depth is:

$$\delta=(2\pi f \sigma \mu)^{-\frac{1}{2}} \tag{7}$$

where:

f=frequency in Hz

15   σ=conductivity of the conductor in mhos/m

μ=permeability in Henrys/m

As can be seen from the equation (7) the frequency increases the skin depth decreases.

20   When track width is increased beyond 10-15 μm the skin effect causes the series resistance of a spiral inductor to increase at high frequencies. Thus, Q is reduced even though a wide track has been used. This trend tends to limit the maximum Q achievable in integrated spiral inductors.

25   Reduced Q at high frequencies in spiral inductors having a wide track width tends to be caused by eddy currents induced in a spiral inductor's inner sections 2812. Multiple narrow tracks placed side-by-side 2804, 2806 tends to reduce the eddy currents produced. In a spiral inductor eddy currents tend to produce a

30   magnetic field opposing a desired magnetic field that produces a desired inductance. Thus, by reducing the eddy currents the desired inductance is more efficiently produced with less loss, hence raising the inductor's Q.

The multi-track technique is advantageously utilized in

35   applications requiring a winding. Examples of devices utilizing

1   36664/PBH/B600 (BP 1298)

multi-track windings comprise: planar spiral inductors (rectangular, octagonal or circular patterns) transformers, and
5   baluns. These devices are suitable for incorporation into architectures comprising: integrated circuits, hybrid circuits, and printed circuit boards.

The first exemplary embodiment shown in FIG. 28a is of a square spiral inductor 2800 that is wound in two turns with
10   several narrow tracks 2804, 2806 disposed in parallel upon a substrate 2802. Equivalently any number of track may be used to achieve a multi-track design. A turn is counted each time the track is wound around in a spiral such that a starting point 2814 is passed. Typically 5 to 20 turns are utilized in a spiral,
15   with 3 to 10 producing optimum performance. Alternative embodiments of the invention equivalently utilize one or more turns as required to achieve a desired inductance for a given track width.

For example a single track spiral inductor is designed to
20   have a single track width of 30 µm in a given number of turns to produce a desired inductance. By splitting an exemplary 30 µm wide track into two 15 µm tracks 2804, 2806 disposed in parallel on the substrate, the inductor Q tends to increase. A typical Q for the single track inductor with a track-width of 30 mm is
25   5.14. The Q of the exemplary dual track inductor 2800 with two 15 mm tracks 2804, 2806 in parallel is typically 5.71. Thus, utilizing two narrower tracks in parallel tends to yield an improved Q over a single wider track. A typical improvement in Q for splitting an inductor's track is in excess of 10%. A further
30   splitting of an inductor's tracks into multiple narrower parallel tracks tends to further increase the measured Q.

FIGS. 28b-28g illustrate various planar devices comprising inductor 2820, 2822, 2824, 2816 and transformer 2826, 2818 configurations suitable for incorporating multiple tracks into
35   their designs. The devices are shown with single tracks for

-75-

clarity. However, it is understood that each of the tracks shown in the devices may comprise multiple tracks constructed as

5   described below. The method is advantageously used in, various planar inductor topologies comprising square 2820, octagonal 2822, and circular 2824.

An example of a 3-turn symmetric inductor is shown 2816. Each of the single tracks shown is sub-divided into multiple

10   tracks as described below. The multiple tracks are joined only at the ends 2826. A series of phantom lines 2828 indicate tracks on a different layer, connected to a track shown by a solid line using one or more vias. When routing multiple vertical tracks 2825 that are tied in common with vias 2827 to a different layer

15   the tracks being routed may be reduced to one track 2829, or the multiple vertical structure may be maintained 2831. This method is suitable for suitable for symmetric inductors of any number of turns.

The symmetric inductor 2816 may be used as a building block

20   to construct a transformer 2818. A second symmetric inductor 2833 is wound in parallel with the symmetric inductor shown 2816. The ends of the first inductor 2830, 2832 are kept separate from the second symmetric inductor 2834, 2836. The resulting four ends 2830, 2832, 2834, 2836 comprise the transformer connections.

25   The symmetric inductor with a parallel winding 2818 is suitable for use as a balun for converting single-ended signals to differential signals and vice versa. The coupling is provided by the winding arrangement.

Alternatively two symmetric inductors of the type shown 2816

30   are placed substantially on top of each other, on different layers to produce a transformer, or balun as previously described.

FIG. 28h is an illustration of a second embodiment of an inductor having a single winding comprising five tracks 2838 per

35   layer. The tracks are a maximum of 5 µm wide. The embodiment

comprises one or more layers. The second embodiment further comprises a square spiral form factor constructed from five

5   conductive tracks 2838 per layer formed into a single turn. Individual tracks are kept at a maximum width of 5 μm. A 0.6 μm gap between adjacent tracks 2840 is maintained. The minimum gap is a requirement for a given process. Here it is a limitation of the CMOS process. At frequencies between 2 GHz and the

10 inductor's self-resonant frequency an inductor constructed of multiple tracks of widths up to the maximum width tends to exhibit improved performance in quality factor (Q). Utilizing multiple narrower tracks in parallel tends to yield an improved Q over a single wider track, and a single double track inductor.

15 The tracks in each layer are connected at their ends by a conductive strip 2842.

In a third exemplary embodiment six tracks are disposed on a layer. In the embodiment, a 30 mm track inductor is split into six parallel tracks of 5 mm each. Utilizing 6 tracks tends to

20 improve the Q from 5.08 to 8.25, a 62% increase in Q. Improvements in an inductor's quality factor tends to improve the suitability of spiral inductors for use in high frequency circuits. For example multi-track spiral inductors are advantageously used in high frequency voltage-controlled

25 oscillator (VCO) and tuned amplifier circuits.

FIG. 28i illustrates the placement of tracks 2844, 2848 in a layered structure 2846. In constructing an inductor according to this technique a set of parallel tracks 2844, 2848 are disposed side-by-side in a arraignment similar to that of coupled

30 transmission lines. The side by side pattern is disposed in multiple layers M5, M4, M3. Each track disposed in a common layer has a starting point and an ending point. Each track's starting point 2850 in a layer is coupled together, and each track's ending point is coupled together in the layer 2852. A

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pass through track 2854 is disposed in a layer to provide access to the end of an inner turn.

5   The placement of conductive via holes V2, V3, V4 in the embodiments of the invention couple the tracks in adjacent layers M2, M3, M4, M5. In the multiple track inductors described, the multi-tracks are joined together at the beginning of a winding 2850 and again joined together at the end of the winding 2852 by

10 a conductive material. Vias between layers are formed to couple a bottom track to one or more tracks disposed in layers above it. Vias are utilized along the length of the track.

      Thus, by utilizing this technique a group of multiple tracks are formed in a first embodiment by disposing tracks in a

15 combination of vertical layers M2, M3, M4, M5 and side-by-side in the same layer 2856, 2858. In a second embodiment an inductor is formed by disposing tracks side by side in the same layer. In a third embodiment an inductor is formed by layering tracks on top of each other vertically. By connecting the track layers

20 vertically using vias, the series resistance loss tends to be decreased due to increased conductor thickness.

      For example, in an embodiment three layers are utilized in which individual track width is limited to 5 to 6 μm in width, with four to six tracks disposed in parallel in each layer. In

25 the embodiment vias are used vertically between metal layers to connect the tracks. The vias are used in as many places as possible along the length of each track to couple the layers. However, the parallel tracks in the same layer are joined to each other only at the ends.

30   FIG. 28j is an illustration of an embodiment utilizing a shield 2860 disposed beneath an inductor 2862. A shield tends to double inductor Q in the 3~6 GHz frequency range for a lightly doped substrate, such as is utilized in a non-epi process, a 100% improvement. If a heavily doped substrate, such as is found in

35 an epi-process is utilized, the shield tends not to improve

inductor Q. The embodiment shown utilizes an n^+ shield 2860.
An n+ diffusion advantageously tends to possess less capacitance

5   between the inductor and ground plane than if polysilicon is used
as the shield material.   The ground planes are silicided
n^+ material possessing a low resistivity. Silicided n^+ material
is available in the fabrication process utilized in CMOS.

FIG. 28k is an illustration of a patterned shield 2864 that

10   is utilized beneath a multi-track inductor.   A patterned n^+
shield is utilized beneath the inductor to reduce losses to the
substrate.   In the embodiment an n+ diffusion is provided in a
fingered pattern of n+ regions 2866. Polysilicon is disposed in
a series of gaps 2868 between the n+ fingers. The patterned

15   shield provides shielding equivalent to a solid ground plane, but
without undesirable eddy currents. The shield is disposed in a
fingered pattern 2866 to prevent having a single large surface
as a ground plane. Fingering tends to prevent the inducement of
eddy currents flowing in one or more ground loops. Ground loops

20   tend to cancel the inductance produced in the spiral.

The finger structure of the patterned shield is constructed
from an n^+ diffusion layer. The gaps between the fingers are
filled with polysilicon material. The n^+ diffusion fingers and
polysilicon fingers formed by the filling are not coupled to each

25   other, thus preventing eddy current flow in the shield.
An interdigitated shield 2864 as described above tends to be an
improvement over an n^+ only shield 2860 of FIG. 28j.   The
interdigitated n+ finger shield also tends to be an improvement
over a higher capacitance fingered polysilicon shield having gaps

30   between the fingers, which is known in the art.

The individual fingers of like material are connected 2870.
To suppress eddy currents and break ground loops care is taken
in the connection of individual fingers 2886 in a ground shield
pattern. The ends of the fingers in a row are connected by a

35   conductive strip of metal 2870. This connection is repeated at

each grouping. The groupings are connected 2870 to a single ground point 2874. In an embodiment a ring of conductive
5   material is disposed on the substrate to connect the finger patterns.

A cut 2876 in the ring is added to suppress ground loop currents. The cut maintains a single point ground by only allowing the flow of current in one direction to reach the single
10   point ground 2874.

One or more spirals of metal have a series resistance associated with them. A spiral can be quite long, thus, the series resistance of the inductor is not negligible in the design of the circuit even with a parallel connection of tracks. As the
15   temperature of the circuit rises, such as would occur after the initial power-up of an integrated circuit, the series resistance of the inductor increases, thus causing the Q to decrease. Circuitry is provided to continuously compensate for this increasing series resistance.

20   An inductor, or coil, has always been a fabrication problem in integrated circuitry. Inductors are typically not used in integrated circuits due to the difficulty of fabricating these devices with high Q's and due to the large amount of area required to fabricate them.

25   It is a rule of thumb that the higher the frequency the smaller the dimensions of the integrated circuit component required in a filter to achieve a given set of circuit values. A spiral inductor of the type described in the embodiments of the invention allows an inductor with improved Q's to be
30   satisfactorily fabricated on a CMOS substrate. Many alternative embodiments of the spiral are known to those skilled in the art. The realization of inductance required in any embodiment of the invention is not limited to a particular type of integrated inductor.

35

The details of multi-track spiral inductor design are
disclosed in more detail in U.S. Patent Application
5   No. 09/493,942 filed January 28, 2000, (B600:36491) entitled
"Multi-Track Integrated Spiral Inductor" by James Y.C. Chang;
based on U.S. Provisional Application No. 60/117,609 filed
January 28, 1999 (B600:34072) and U.S. Provisional Application
No. 60/136,654 filed May 27, 1999 (B600:34676), the subject of
10   which is incorporated in this application in its entirety by
reference.

FIG. 29 is an exemplary illustration of the possible effects
of inductor Q on filter selectivity in a parallel LC circuit,
such as shown in 2706 of FIG. 27. The Q of a spiral inductor
15   tends to be low. In order to advantageously control the Q so
that the maximum performance of an integrated filter may be
obtained, calibration of inductor Q is used.

The overall effect of this is that when a device with high
series resistance and thus, low Q is used as a component in a
20   filter that the overall filter Q is low 2902. A high Q filter
response is sharper 2984. The goal of a filter is to achieve
frequency selectivity. The filter selectivity is the same
electrical property as selectivity in the "front end" of the
receiver previously described. If the filter has a low Q
25   frequencies outside the pass band of the filter will not achieve
as great of an attenuation as if the filter contained high Q
components. The high degree of selectivity is required to reject
the multitude of undesirable distortion products present in a
receiver that fall close to the tuned signal. Satisfactory
30   inductor dimensions and device Q have been obstacles in
integrating filters on a CMOS substrate.

Prediction of the inductance yielded by the spiral is
closely approximated by formula. However, prediction of the
inductor's Q is more difficult. Three mechanisms contribute to
35   loss in a monolithically implemented inductor. The mechanisms

are metal wire resistance, capacitive coupling to the substrate, and magnetic coupling to the substrate. Magnetic coupling
5   becomes more significant in CMOS technologies with heavily doped substrates, because the effect of substrate resistance appears in parallel with the inductor. The first four or five turns at the center of the spiral inductor contribute little inductance and their removal helps to increase the Q. In spite of extensive
10 research inductors implemented in CMOS possess Qs after limited to less than five.

FIG. 30 is an illustration of a typical filter bank 3002 utilized in embodiments of the invention for filtering I and Q IF signals 3208. Band pass filters utilized in the embodiments
15 of the invention have a center frequency f_c and are designed to provide a given selectivity outside of the pass bond. The exemplary filters 3002 also incorporate gain. Gain and selectivity are provided by an amplification ("transconductance") stage with an LC load, resulting in an active filter
20 configuration that gives the filter response shown. Selectivity is provided principally by the LC load. The gain is attributable to the transconductance stage. The transconductance stage comprises a linearized differential pair amplifier that has an improved dynamic range. Over temperature the filter response
25 degrades as indicated in FIG. 30. This degradation is typically attributed to inductors.

With the spiral inductors utilized in the embodiments of the invention the gain of this filter stage is substantially determined by the Q or quality factor of the inductor. The Q is
30 in turn substantially determined by the series resistance of the metal in the spiral of the inductor. The Q decreases as temperature increases causes an increase in inductor series resistance. The decrease in Q with increasing temperature adversely affects the filter characteristics. As can be seen in

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306 at FIG. 30 as the temperature increases from 50°C 3004 to 100°C 3006 overall gain decreases, and selectivity is degraded.

5

ACTIVE FILTER UTILIZING A LINEARIZED DIFFERENTIAL PAIR AMPLIFIER

A linearized differential pair amplifier is used in the active filters present in the receiver. The technique utilized to linearize the CMOS differential pair described in light of application to active filters may be utilized in any application in which a differential amplifier having a linear response is desirable.

FIG. 31a is a diagram of an exemplary differential transconductance stage 3102 with an LC load 3104. Together the transconductance stage and LC load make up a filter 3002 that is a part of filter bank 3001. The exemplary embodiment of the filter is disposed on a CMOS substrate that is part of an integrated receiver.

FIG. 31b is a block diagram of a linearized differential pair amplifier that is coupled to distortion canceling linearization circuit. Gain stage 3102 comprises a differential pair amplifier 3103 that has a linearization circuit 3105 coupled to form a linearized differential pair. In the embodiment shown the linearization circuit is coupled in parallel to the differential pair amplifier.

The linearized differential pair typically improves maximum signal handling capability over that of a differential pair in excess of 19 dB. In the past, typical improvements with prior art linearization schemes applied to differential pair amplifiers tended to be around 7 dB. Thus, the approach described in the embodiment tends to have a dynamic range advantage of 12 dB over the prior art.

An embodiment of the differential pair amplifier 3103 comprises a first and second FET transistor M1, M2. Equivalently, other type of transistor are contemplated as satisfactory

substitutes. A differential input comprises signals V_{i1} and V_{i2}

coupled to the inputs of the amplifier 3103 and linearization

5   circuit 3105. A differential output comprises signals V_{o1} and V_{o2}.

An embodiment of the linearization circuit 3105 comprises

two or more auxiliary differential pairs 3107, 3109 respectively.

Each auxiliary differential pair comprises a first and a second

FET transistor. Auxiliary differential pair 3107 comprises

10   transistors M3 and M4. Auxiliary differential pair 3109 comprises

transistors M5 and M6. Equivalently, other type of transistor are

contemplated as satisfactory substitutes. Further improvements

in linearization is possible by adding more auxiliary

differential pairs. However, as linearization is increased the

15   size of transistors contained in the additional auxiliary

differential pairs decreases. Thus, a limit in the linearization

that may be obtained is set by the practical aspects of device

matching and scaling.

FIG. 31c is an illustration depicting a representative

20   channel of any one of the typical field effect of transistors M1,

M2, M3, M4. A channel of length l, and a width w and a thickness

t is disposed on a substrate to form a field effect transistor

(FET) as shown in FIG. 31c. The channel is provided with ohmic

contacts 3111 for a drain connection and a source connection.

25   In an exemplary embodiment of a filter designed to operate

at 275 MHz the channel lengths of M1, M2, M3, M4, M5, and M6 were

chosen to have $l = 0.6$ μm. In Table I for an $I_{ss} = 9$ mA and n = 16

the channel widths for the transistors in the exemplary

embodiment of the 275 MHz filter are shown.

30

Device Width				
$W_{1,2}$	$W_{4,5}$	$W_{3,6}$	Iss	n
1.9um x 20	2um x 5	1.95um x 2	9mA	16

35   Table I

The subscripts in table I refer to the transistor that is associated with a given channel width. For example $W_{1,2}$ refers to

5   the channel width of transistor M1 and M2. I_{ss} is the main pair tail current source, and n refers to the ratio of the main pair tail current source.

Transistor M1 and M2 has a width of 1.9 μm x 20, transistor M4 and M5 have a channel width of 2.0 μm x 5, and transistors M3

10   and M6 have a channel width of 1.95 μm x 2. In the notation used the dimension with an "x" refers to the number of transistors coupled in parallel. For example 2.0 μm x 5 refers to 5 transistors with a 2 μm channel width coupled in parallel, to form an overall 10 μm channel width. An exemplary filter

15   constructed with these channel widths and the fixed length exhibits a third order intermodulation typically less than -70 dB when fed with a two-tone input, each tone having a magnitude of 125 mV_p.

The channel widths and lengths of the exemplary embodiment

20   were chosen through an optimization process. The transistors in the auxiliary differential pair amplifiers, when stimulated by the amplifier input will produce a signal that when added to the gain stage output, will tend to reduce distortion.

FIG. 31d is a block diagram showing the interconnection of

25   a differential pair amplifier 3103 to a linearization circuit 3105. Gain stage 3103 is made up of a differential pair amplifier comprising a pair of transistors M1 and M2, each transistor having a drain, a source and a gate. Transistors M1 and M2 tend to contribute to the majority of an overall amplifier

30   gain produced.

In the differential pair amplifier the sources of M1 and M2 are each coupled to a first terminal of a current source I_{ss}. A second terminal of I_{ss} is coupled to ground. Current source I_{ss} is a conventional current source implemented in a manner known to

35   those skilled in the art. The drain of M1 is coupled to an

output current I_1.   The drain of M2 is coupled to an output comprising current I_2.   A differential input voltage is applied across a pair of terminals V_{-1}, V_{12} that are coupled to the gates of M1 and M2, respectively.

The two auxiliary pair differential amplifiers 3107, 3109 are present as shown. The auxiliary amplifiers tend to linearize the currents I_1 and I_2.   Currents 3113 and 3115 tend to subtract non-linear currents from current I_1 and current I_2 respectively. The gates of the differential pairs 3107, 3109 are also driven by the input differential voltage that is supplied to the differential pair amplifier 3103.

The relationship of transistor parameters of channel length and width (of FIG. 31c) in transistors M1, M2 to the transistor parameters of M3, M4, M5, M6, contained in the auxiliary differential pair amplifiers 3107 and 3109 of the linearization circuit, is to minimize distortion. The transistors function in relation to each other such that distortion created by the transistors in the differential pair amplifier generating current outputs I_1 and I_2, tends to be reduced by the currents generated by the transistors M3, M4, M5, M6 of the auxiliary differential pair amplifiers 3113, 3115. In order to select appropriate transistor parameters a new CMOS differential pair linearization technique is utilized. The technique is found from examining the operating parameters of a differential pair amplifiers and cross coupled differential pair amplifiers.

FIG. 31e is a schematic illustrating a CMOS differential pair of transistors. In the exemplary embodiment the transistors are biased to operate in the saturation region. The differential pair of transistors generate a differential current output I_{d1} and I_{d2}, that is proportional to a differential input voltage, supplied by a pair of voltages V_{11} and V_{12} as referenced to a circuit ground potential. The differential pair of transistors is comprised of a first transistor M1 and a second transistor M2.

Each transistor M1, M2 has a drain, a source and a gate
terminal. The sources of M1 and M2 are coupled to a first
5   terminal of a current source I_{ss}. The current source I_{ss} has a
second terminal which is coupled to the circuit ground. Current
source I_{ss} is constructed conventionally as is known to those
skilled in the art. The voltages V_{i1} and V_{i2} are applied to the
gates of transistors M1 and M2 respectively. The drains of
10   transistors M1 and M2 supply the current outputs I_{d1} and I_{d2}
respectively.

The differential pair of FIG. 31e is biased so that each
transistor M1 and M2 operates in the saturation region defined
by $(V_{GS} - V_{tn})_{M1,2} \le V_{DS}$ for each transistor M1 and M2. Derivation of
15   this relationship is disclosed in "Analysis and Design of Analog
Integrated Circuit Design", by P.R. Gray and R.G. Meyer, 3rd ed.
John Wiley and Sons, 1983, the disclosure of which is herein
incorporated in its entirety by reference. Where V_{GS} is a gate
source voltage as measured across the gate and source terminals
20   of M1 and M2, V_{DS} is a drain source voltage as measured across
the drain and source terminals of M1 and M2, and V_{th} is a
threshold voltage associated with M1 and M2. A derived term V_{gt}
is defined in conjunction with equation (7.1) and is equal to on
$V_{gs}-V_{th}$. The superscript notation M1,2 associated with V_{gt}
25   indicates the parameter is associated with transistors M1 and M2.
When the differential pair shown in FIG. 31e is biased in the

30

35

saturation region the current and voltage relationship is given by equation (7.1).

$$\Delta I_d = I_{ss} \times \frac{\Delta V_i}{V_{gt}^{M1,2}} \times \left\{ 1 - \frac{1}{4}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^2 \right\}^{0.5} \quad for \quad \Delta V_i \leq \sqrt{2} \times V_{gt}^{M1,2} \qquad (7.1)$$

where:

$$\Delta I_d = I_{d1} - I_{d2}$$

$$\Delta V_i = V_{i1} - V_{i2}$$

$$V_{gt}^{M1,2} = \left(V_{GS} - V_{tn}\right)_{M1,2} \quad @ \quad \Delta V_i = 0$$

Note that ΔV_i denotes the peak signal level for each of the two signals.

A series expansion for $(1-x^2)^{0.5}$ is applied to equation (7.1) to obtain equation (7.2) as a current output defined in terms of a sum of a series of input voltages each raised to progressively greater exponential powers.

$$\Delta I_d = I_{ss} \times \left\{ \left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right) - \frac{1}{8}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^3 - \frac{1}{128}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^5 - \frac{1}{1024}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^7 \cdots \right\} \quad (7.2)$$

For small input signals ΔV_i satisfying the condition, $\Delta V_i \ll \Delta V_{gt}^{M1,2}$, the first linear term of equation 2 is much larger compared to the higher order terms. Under this condition, the output current ΔI_d is almost a linear function of input voltage ΔV_i.

However, as the input signal level approaches $V_{gt}^{M1,2}$ higher order terms tend to contribute more to the output current. The contribution of the higher order, nonlinear terms gives rise to spurious harmonic components and intermodulation distortion

(IM3). Thus the differential amplifier behaves linearly for small input signals and begins to distort when large signals are
5   applied.

In filter design the more significant spurious response tends to be third order intermodulation distortion. The following process for minimizing distortion is carried out by considering only intermodulation distortion present in a
10 differential pair amplifier.

For the differential pair of FIG. 31e, third order intermodulation distortion (IM3) is given in equation (7.6).

To calculate IM3, the coefficients in the following equation must first be found:
15

$$\Delta I_d \;=\; a_1 v_1 \;+\; a_2 v_1^{\,2} \;+\; a_3 v_1^{\,3} \;+\; a_4 v_1^{\,4} \;+\; a_5 v_1^{\,5} \;+\; a_6 v_1^{\,6} + \ldots \ldots \tag{7.3}$$

20 Where v_1 denotes the input voltage.
By comparing equation (7.3) to equation (7.6) the coefficients of equation (7.3) are determined:

$$a_1 = \frac{I_{ss}}{(V_{GS} - V_{th})} \qquad a_2 = 0$$
25

$$a_3 = -\frac{I_{ss}}{8\,(V_{GS} - V_{th})^3} \qquad a_4 = 0 \tag{7.4}$$

30 $$a_5 = -\frac{I_{ss}}{128\,(V_{GS} - V_{th})^5} \qquad a_6 = 0$$

The third order intermodulation components IM3, are known to be generated by the odd coefficients Thus, by collecting the terms
35 having odd coefficients, and defining their sum to be the third

order intermodulation ("IM3") the following equation (7.5) is
obtained.

5   Peak input voltage is denoted by a caret over the letter $\hat{v}_1$.

$$IM3 \approx \frac{3}{4}\frac{a_3}{a_1}\hat{v}_1^2 + \frac{25}{8}\frac{a_5}{a_1}\hat{v}_1^4 + \cdots\cdots \tag{7.5}$$

10

Inserting the values for a_1 and a_3 and a_5 from eq 4.22 into
equation (4.23) yields an expression for third order
15   intermodulation (IM3) that is expressed in terms of a
differential pair amplifiers transistor parameters.

$$IM_3 \approx \frac{3}{32}\times\left(\frac{\Delta V_1}{V_{gt}^{M1,2}}\right)^2 + \frac{25}{1024}\left(\frac{\Delta V_1}{V_{gt}^{M1,2}}\right)^4 + \frac{735}{2^{16}}\left(\frac{\Delta V_1}{V_{gt}^{M1,2}}\right)^6 + \cdots\cdots \tag{7.6}$$

20

The ΔV_1 of FIG. 31e denotes peak signal level for each of
25   the two input signals.

A large signal transconductance ("G_n") is the rate of change
of input current (ΔI_d) with respect to the rate of change of the
input voltage (ΔV_1). Large signal transconductance is found by
differentiating equation (7.2) with respect to ΔV_1 to yield an
30   expression for large signal transconductance.

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$$G_m = \frac{d\Delta I_d}{d\Delta V_i}$$

$$\approx \frac{I_{ss}}{V_{gt}^{M1,2}}\left\{1 - \frac{3}{8} \times \left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^2 - \frac{5}{128}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^4 - \frac{7}{1024}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^6 \cdots\cdots\right\} \qquad (7.7)$$

10

The first term of equation (7.7) represents a small signal transconductance ("g_m"):

15
$$g_m = \frac{I_{ss}}{V_{gt}^{M1,2}} \qquad\qquad (7.8)$$

A deviation of large signal transconductance (G_m) from small
20 signal transconductance (g_m) is defined to be:

$$\frac{\Delta G_m}{g_m} \approx -\frac{3}{8} \times \left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^2 - \frac{5}{128}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^4 - \frac{7}{1024}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^6 \cdots\cdots \qquad (7.9)$$

25

Transconductance variations are given by equation (7.9)
which represents a fractional change in transconductance for
variations in input signal level.

By examining the equations derived for relatively small
30 signals, a relationship between two of the equations is noted.
There is a relationship between the equation for third order
intermodulation distortion and the equation for transconductance
variations. The equations have common terms, and are directly
proportional to each other. For a given input level, on
35 examining equations and the third order intermodulation

distortion level of equation (7.6) is approximately one-quarter
of the transconductance variations of equation (7.7). This
5   relationship for small signals is expressed in equation (7.10):

$$IM_3 \approx \frac{1}{4} \times \frac{\Delta G_m}{g_m} \qquad for \qquad \Delta V \ll V_{gt}^{M1,2} \qquad\qquad (7.10)$$

10

The relationship in equation (7.10) suggests that third
order intermodulation distortion is controlled by controlling
variations in transconductance that typically occur when the
input voltage changes. Thus, to a first order of approximation,
15 minimization of transconductance variations over a range of input
signal levels tends to reduce third order intermodulation
distortion (IM3). The minimization of transconductance variations
is found by applying calculus to minimize the functional
relationship.

20   FIG. 31f is a graph of a differential current $(\Delta I_{1,2}=\Delta I_d)$ and
normalized transconductance (G_m/g_m) as input voltage $(V_{in}=\Delta V_-)$ is
varied in the differential pair of FIG. 31e. From this curve an
exemplary baseline intermodulation distortion for an
uncompensated differential pair amplifier of FIG. 31e is found.
25 In creating this graph values of, $V_{gt}^{M1,2} = 0.7V$ and $I_{ss} = 2.4mA$ were
used. The graph shows the increasing non-linearities present in
the output current $(\Delta I_{1,2}=\Delta I_d)$as the input voltage $(V_{in}=\Delta V_-)$
driving the amplifier increases.

For an input voltage of 250mv the large signal
30 transconductance is .96 times the small signal transconductance
3117. Thus, $\Delta G_m/g_m \approx 0.04$. By substituting .04 into equation (7.10)
the third order IM level is 1/100, or -40 dB (-40=20Log (1/100)).
A differential pair amplifier comprises a baseline from which
improvements in linearity are measured.   Interconnected

35

linearizing circuitry is next added to the differential pair
amplifier of FIG. 31e to improve its linearity.

5   FIG. 31g is a schematic diagram of a differential pair
amplifier 3127 with a second cross coupled differential pair
error amplifier 3129 added that tends to reduce distortion.

Linearity of a differential pair amplifier may be improved
by using large values of an applied gate overdrive voltage
10   $(V_{GS} - V_{tr})_{M1,2}$ that is applied to transistors M1 and M2.
A limiting factor in utilizing large values of gate overdrive
voltage is a maximum available supply voltage. With a reduced
scaling of device sizes common in today's more compact circuit
layouts, a maximum available supply of voltage tends to be
15   reduced. Since a higher voltage required for a gate overdrive
condition is not present, alternative linearization techniques
are desirable. One technique is the addition of a cross-coupled
differential pair 3129, that functions as an error amplifier, to
a differential pair amplifier 3127.

20   A preferable linearization process takes the form of adding
error currents I_{a3} I_{a4} to differential amplifier currents I_{d1} I_{d2}
in a way that tends to improve the linearity of output currents
3131 3133. The error currents I_{d3} and I_{a4} are subtracted tend to
become non-linear more rapidly than the currents of the
25   differential pair amplifier I_{d1} and I_{a2}.

Subtraction is achieved by cross coupling the amplifiers
3127 and 3129. A differential signal may be referenced to ground
by considering it to be made up of two signals. The equivalent
signal is a set of two individual signals, 180 degrees out of
30   phase and of equal amplitude referenced to ground. In a
differential voltage signal the voltages have opposite polarities
of equal amplitude at any given time.

In a differential current signal the currents flow in
opposite directions and are of equal magnitude at any given time.
35   In the case of a current one signal flows into the terminal, the

other out of it. If the two differential signals are coupled to
the same terminal the resultant signal would be canceled since
5   each signal is equal and opposite.   If the signals are unequal
the cancellation is not total.

Thus, by cross coupling the differential pair amplifier 3127
to the error amplifiers 3129 in parallel the currents I_{d3} I_{d4}
present in each drain of the error amplifier are coupled to the
10   drain currents I_{d2} I_{d1} of the differential pair amplifier
respectively. Paired signals I_{d3} I_{d2} and I_{d4} I_{d1} are 180 degrees out
of phase and unequal in amplitude, causing a subtraction of The
error amplifier current from the differential pair amplifier
current in each lead.

15   The differential pair amplifier 3127 has a differential
input V_{i1} and V_{i2}.   The differential pair amplifier has a
differential current output provided by currents 3131 and 3133.
By Kirchhoff's current law the current 3133 flowing out of node
3121 is equal to a sum of branch currents I_{d3} and I_{a2} into node
20   3121. Similarly, current 3131 flowing out of node 3119 is equal
to a sum of branch currents I_{d1} and I_{d4} flowing into node 3119. To
provide the branch currents a main differential pair 3127 and an
auxiliary differential amplifier alternatively termed an error
amplifier 3129 are provided.

25   The main differential pair 3127 comprises transistors M1 and
M2.   The gates of transistors M1 and M2 are driven by
differential input voltage V_{i1} and V_{i2}. The sources of M1 and M2
are coupled to a first terminal of a conventional current source
I_{ss} A second terminal of I_{ss} is coupled to ground. The drains of
30   M1 and M2 provide output currents I_{d1} and I_{d2}, respectively.

The auxiliary cross-coupled differential pair 3129 comprises
transistors M3 and M4. The gate of M3 is coupled to the gate of
M1, and the gate of M4 is coupled to the gate of M2. The sources
of M3 and M4 are coupled together. The coupled sources of M3 and
35   M4 are in turn coupled to a first terminal of a current source

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I_{ss}/n. Current from source I_{ss}/n is a fraction of I_{ss} in order to control the current output I_{d3} I_{d4} of The auxiliary amplifier. A

5   second terminal of I_{ss}/n is coupled to ground. The drain of M3 is coupled to the drain of M2. The drain of M4 is coupled to the drain of M1. This connection of gates and drains creates the desired cross coupling.

The current and voltage relationships in the cross coupled
10   differential amplifier are as follows:

where:

$\Delta I_d^{1,2}$ =

$\Delta I_d^{3,4}$ =   (7.11)

15

$\Delta I_{Total} = \Delta I_d^{1,2} - V I_d^{3,4}$

The $\Delta I_d^{1,2}$ is given by:

20

$$\Delta I_d^{1,2} = \Delta I_d = I_{d1} - I_{d2}$$

$$= I_{ss} \times \left\{ \left(\frac{\Delta V_1}{V_{gt}^{M1,2}} \right) - \frac{1}{8} \left(\frac{\Delta V_1}{V_{gt}^{M1,2}} \right)^3 - \frac{1}{128} \left(\frac{\Delta V_1}{V_{gt}^{M1,2}} \right)^5 - \frac{1}{1024} \left(\frac{\Delta V_1}{V_{gt}^{M1,2}} \right)^7 \ldots\ldots \right\} (7.12)$$

25

The $\Delta I_d^{3,4}$ is given by:

$$\Delta I_d^{3,4} = I_{d3} - I_{d4}$$

30 $$= \frac{I_{ss}}{n} \times \left\{ \left(\frac{\Delta V_1}{V_{gt}^{M3,4}} \right) - \frac{1}{8} \left(\frac{\Delta V_1}{V_{gt}^{M3,4}} \right)^3 - \frac{1}{128} \left(\frac{\Delta V_1}{V_{gt}^{M3,4}} \right)^5 - \frac{1}{1024} \left(\frac{\Delta V_1}{V_{gt}^{M3,4}} \right)^7 \ldots\ldots \right\} (7.13)$$

35

5   Assuming that $\dfrac{V_{gt}^{M1,2}}{V_{gt}^{M3,4}} = m$ and thus $\dfrac{W^{M1,2}}{W^{M3,4}} = \dfrac{n}{m^2}$, the total current is found to be:

$$\Delta I_{Total} = I_{ss} \times \left\{ \left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)\left(1 - \frac{m}{n}\right) - \frac{1}{8}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^3\left(1 - \frac{m^3}{n}\right) - \frac{1}{128}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^5\left(1 - \frac{m^5}{n}\right) \right.$$
$$\left. - \frac{1}{1024}\left(\frac{\Delta V_i}{V_{gt}^{M1,2}}\right)^7\left(1 - \frac{m^7}{n}\right)\ldots\ldots \right\} \quad (7.14)$$

15   Where the ration of the channel widths comes from the current
     sources having a ratio of n, and the v_{gt}s have a ratio of m.
     Thus, for a MOS transistor operating in saturation:

20   $$I_{ds} = \frac{\mu Cox W}{2L}\left(V_{gs} - V_{tr}\right)^2 \qquad (7.15)$$

$$\frac{I_{ds}^{M1,2}}{I_{ds}^{M3,4}} = \frac{W^{M1,2}\left(\left(V_{gs} - V_{tn}\right)^2\right)^{M1,2}}{W^{M3,4}\left(\left(V_{gs} - V_{tn}\right)^2\right)^{M3,4}} \qquad (7.16)$$

25

     $$-> \frac{W^{M1,2}}{W^{M3,4}} = \frac{n}{m^2} \qquad (7.17)$$

30

     The third order term of equation (7.14) that controls the
     contribution of third order intermodulation goes to zero when
     $m^3/n = 1$. The cross coupled differential amplifier is described
     . in more detail in P.R. Gray and R.G. Myer, "*Analysis and Designs
35   of Analog Integrated Circuit Design,*" Third Edition, John Wiley

& Sons, 1993. Utilizing a value of n = 9.5 and m = 2, a dynamic range of the input to the amplifier is increased by 6.5 dB, for

5   an IM3 level of - 40 dB. Where n is the ratio of current source values, and the ratio of m to n was previously defined.

The dynamic range of the input to maintain a -40dB third order intermodulation level may be further extended. Extension of dynamic range is possible by using two or more differential

10   pairs cross-coupled in parallel to a main differential pair. In an embodiment, the main differential pair has two auxiliary differential pairs associated with it to linearize the main differential pairs output.

FIG. 31h is a graph illustrating The linearized output

15   current of a cross coupled differential output amplifier. The auxiliary differential pair amplifier 3129 of FIG. 31g subtracts a small current I_{a3}, I_{a4} from the output current of the differential pair amplifier $\Delta I_d^{3,4}$. The currents I_{d3}, I_{d4} are subtracted from The output currents I_{d1} and I_{d2}, respectively.

20   This small amount of current tends to become nonlinear more rapidly than $\Delta I_d^{1,2}$.

The derivation above for the circuit of 31h utilized a ratio of channel widths to adjust The proper error amplifier currents to cancel the third order intermodulation distortion.

25   A chosen channel width for transistors M1 and M2 was selected, and a channel width was found for transistors M3 and M4 that tends to yield an IM3 level of -40dB. This yields an increase in dynamic range of approximately 6.5 dB. Increasing the number of auxiliary differential pairs present and utilizing a

30   linearization optimization process tends to improve overall amplifier linearity.

FIG. 31i is a schematic of a differential pair amplifier 3102 incorporating two auxiliary cross-coupled differential pairs 3107 3109 to improve linearization of the output response I_1 and

35   I_2. The main differential pair 3103 comprises transistors M1 and

M2. The gates of M1 and M2 are coupled to a differential input voltage V_{i1} and V_{i2}. The sources of M1 and M2 are coupled to a

5   first terminal of current source I_{ss}. A second terminal of I_{ss} is coupled to ground. Current source I_{ss} is typically constructed as known to those skilled in the art. The drains of M1 and M2 supply currents I_{d1} and I_{d2}, respectively. The drains of M1 and M2 are coupled to current outputs I_1 and I_2, respectively.

10   The first auxiliary differential pair 3107 comprises transistors M3 and M4. The gate of M3 is coupled to differential input voltage V_{i1}. The gate of M4 is coupled to differential input voltage V_{i2}. The sources of M3 and M4 are coupled together and then to a first terminal of a first current source I_{ss}/n. A

15   second terminal of I_{ss}/n is coupled to a ground potential. Current source I_{ss}/n is typically constructed as a conventional current source as is known to those skilled in the art. The drain of M3 is coupled to the drain of M2. The drain of M4 is coupled to the drain of M1.

20   The second auxiliary differential pair 3109 comprises transistors M5 and M6. The gate of M5 is coupled to differential input voltage V_{i1}. The gate of M6 is coupled to differential input voltage V_{i2}. The sources of M5 and M6 are tied together to a first terminal of a second current source I_{ss}/n. A second

25   terminal of I_{ss}/n is coupled to ground. The source of M5 is coupled to the source of M2. The source of M6 is coupled to the source of M1.

FIG. 31j is a graph of the currents present in the main and two auxiliary differential pair amplifiers graphed against input

30   voltage   as   measured   across   the   input   terminals   where Vin = V_{i1} - V_{i2}. This graph illustrates an offset between currents $\Delta I_{3,4}$ and $\Delta I_{5,6}$. An offset is present where the input voltage passes through zero 3135. The currents $\Delta I_{3,4}$ and $\Delta I_{5,6}$ from the auxiliary differential pair amplifiers are much smaller

35   than the main differential pair amplifier current $\Delta I_{1,2}$. It is

desired to produce an output current that varies a linear
relationship to the input voltage. The differential currents
5   from the auxiliary differential pairs $\Delta I_{5,6}$ and I $\Delta_{3,4}$ are
subtracted from $\Delta I_{1,2}$ to produce curve of total differential
output current ΔI_{Total}.

The composite curve ΔI_{Total} is a more linear curve than $\Delta I_{1,2}$.
Thus, by subtracting the currents produced by the auxiliary
10   differential pair amplifiers, The linearity of The current versus
voltage response is improved. The amount of current produced in
auxiliary cross-coupled differential pairs over a range of input
voltage Vin is related to a transconductance characteristic of
each of a set of transistors in the amplifier.

15   Thus, to shape The ΔI_{Total} curve is necessary to fabricate M3,
M4, M5, and M6 so that the currents they produce will contribute
to The linearization of The ΔI_{Total} curve. Shaping is done through
manipulating transconductance. Transconductance is an inherent
transistor parameter related to drain current I_d. It is defined
20   as follows:

$$g_m = \frac{dI_{\cup}}{dV_{gs}} \qquad\qquad (7.18)$$

25

Thus, by controlling the transconductance of the transistors in
the auxiliary differential pairs, the output current of the main
differential pair is linearized by superposition of the currents.
To reduce third order inter modulation close to zero, a flat G_m
30   curve for the amplifier tends to be advantageous.

FIG. 31k is a graph of transconductance curves for the
differential amplifier made up of a main differential pair
amplifier 3103 and a linearization circuit 3105 comprising
differential pair amplifiers 3107 and 3109. The main
35   differential pair amplifier possesses a transconductance

characteristic shown by the curve $G_m^{M1,2}$ having a peaked response.

To reduce third order air modulation distortion, it is desirable to shape the transconductance curve $G_m^{M1,2}$ so that the peak of is flattened as shown by the curve G_m^{Total}. flattening is accomplished by subtracting or decreasing the G_m in the peak region of the curve. The decrease is achieved by The linearization circuit 3105.

Auxiliary differential pair amplifier 1 3107 exhibits a characteristic transconductance curve centered about a voltage offset V_{os} from zero input volts, and is denoted $G_m^{M3,4}$ on the graph. The transconductance curve for auxiliary differential pair amplifier 2 3109 is offset in the negative direction from zero input voltage by an amount that is equal to the first auxiliary pair V_{os}, this curve is denoted $G_m^{M5,6}$.

FIG. 311 illustrates an equivalent circuit that provides an offset voltage V_{os} that permits shaping of The G_m^{Total} curve. The addition of an offset voltage in The auxiliary differential pair amplifiers allows a more accurate cancellation of non-linearities. The introduction of offset voltage V_{os} is illustrated by the addition of a voltage source in the gate leads of M3 and M6. The voltage source adds in series with The input voltages V_{i1} and V_{i2} to create the offset. The voltage source is shown as a battery. However, the offset voltage is equivalently added in a number of ways comprising building it into the semiconductor circuit parameters and providing biasing circuitry. The offset voltages are built into the circuit by choosing different widths for the auxiliary differential pair devices.

Returning to FIG. 31k, the transconductance curves of the auxiliary differential pairs add to form a G_m curve shown by $G_m^{M3,4} + G_m^{M5,6}$. The composite curve $G_m^{M3,4} + G_m^{M5,6}$ is subtracted from the main differential pair curve $G_m^{M1,2}$ to produce a final composite transconductance curve G_m^{Total} that controls the overall amplifier current response and linearity. The current

relationships for a differential pair amplifier that includes offsets in The linearization circuit are as follows:

5

$$G_m^{Total} = G_m^{M1,2} - \left(G_m^{M3,4} + G_m^{M5,6} \right) \tag{7.19}$$

10   The current in the auxiliary pairs is given by:

$$\Delta I_d^{3,4} = I_{d3} - I_{d4}$$

$$= \frac{I_{ss}}{n} \times \left\{ \left(\frac{\Delta V_1 + V_{os}}{V_{gt}^{M3,4}} \right) - \frac{1}{8} \left(\frac{\Delta V_1 + V_{os}}{V_{gt}^{M3,4}} \right)^3 - \frac{1}{128} \left(\frac{\Delta V_1 + V_{os}}{V_{gt}^{M3,4}} \right)^5 - \frac{1}{1024} \left(\frac{\Delta V_1 + V_{os}}{V_{gt}^{M3,4}} \right)^7 \cdots \cdots \right\} \tag{7.20}$$

20

$$\Delta I_d^{5,6} = I_{d5} - I_{d6}$$

$$= \frac{I_{ss}}{n} \times \left\{ \left(\frac{\Delta V_1 - V_{os}}{V_{gt}^{M5,6}} \right) - \frac{1}{8} \left(\frac{\Delta V_1 - V_{os}}{V_{gt}^{M5,6}} \right)^3 - \frac{1}{128} \left(\frac{\Delta V_1 - V_{os}}{V_{gt}^{M5,6}} \right)^5 - \frac{1}{1024} \left(\frac{\Delta V_1 - V_{os}}{V_{gt}^{M5,6}} \right)^7 \cdots \cdots \right\} \tag{7.21}$$

30

35

And the total current is:

5

$$\Delta I_{Total} = \Delta I_d^{1,2} - \left(\Delta I_d^{3,4} - \Delta I_d^{5,6} \right)$$

$$= I_{ss} \times \left\{ \left(\frac{\Delta V_i}{V_{gt}^{M1,2}} \right) - \frac{1}{8} \left(\frac{\Delta V_i}{V_{gt}^{M1,2}} \right)^3 - \frac{1}{128} \left(\frac{\Delta V_i}{V_{gt}^{M1,2}} \right)^5 - \frac{1}{1024} \left(\frac{\Delta V_i}{V_{gt}^{M1,2}} \right)^7 \cdots \right\}$$

10

$$- \frac{I_{ss}}{n} \times \left\{ \left(\frac{\Delta V_i - V_{os}}{V_{gt}^{M5,6}} \right) - \frac{1}{8} \left(\frac{\Delta V_i - V_{os}}{V_{gt}^{M5,6}} \right)^3 - \frac{1}{128} \left(\frac{\Delta V_i - V_{os}}{V_{gt}^{M5,6}} \right)^5 \right.$$
$$\left. - \frac{1}{1024} \left(\frac{\Delta V_i - V_{os}}{V_{gt}^{M5,6}} \right)^7 \cdots \right\}$$

15

$$- \frac{I_{ss}}{n} \times \left\{ \left(\frac{\Delta V_i + V_{os}}{V_{gt}^{M3,4}} \right) - \frac{1}{8} \left(\frac{\Delta V_i + V_{os}}{V_{gt}^{M3,4}} \right)^3 - \frac{1}{128} \left(\frac{\Delta V_i + V_{os}}{V_{gt}^{M3,4}} \right)^5 \right.$$
$$\left. - \frac{1}{1024} \left(\frac{\Delta V_i + V_{os}}{V_{gt}^{M3,4}} \right)^7 \cdots \right\} \tag{7.22}$$

20

The desired end result is to choose variables Vos, $V_{gt}^{M4,4,5,6}$ and n for equation (7.22) so that a plot of ΔI_{Total} verses V_i results in a straight line. An optimization package to aid

25   calculations is equivalently utilized to determine the desired parameters. A straight line has constant slope. The slope of the line is found by taking the first derivative. For The best possible linearity equation (7.22) is differentiated with respect to input voltage. Equation (7.22) is symmetrical with respect to

30   input voltage. Thus, the even order derivative terms are set to zero when evaluated at zero input voltage. Next, optimal values are derived for the three parameters n, V_{os}, and $V_{gt}^{M3,4,5,6}$. The result is a maximally flat transconductance curve that yields a linear current verses voltage curve.

35

For example in a design that requires an IM3 better than 65 dB is required. From equation (7.10) a transconductance curve to

5   achieve the desired IM3 has a flatness tending to be no greater than +/- 0.25 dB. To find the desired values the optimization process is carried out by inspection coupled with a process of trial and error. In using an iterative optimization process the following values were selected as a starting point:

10

$$V_{gt}^{M3,4} \approx V_{gt}^{M1,2} / 2 \qquad V_{os} \approx V_{gt}^{M3,4} / 3 \qquad\qquad (7.23)$$

15   The offset voltages are built into the integrated circuit by choosing the W/L ratio so that transistors that comprise the same differential pair have differing widths. For example as previously shown in Table I. In the case of a linearization circuit 3105, as shown in FIG. 311 the W/L ratio of M3 and M6 is

20   different from M4 and M5.

$$V_{os} \approx \left(\frac{V_{gt}^{M34}}{2} \right) \times \frac{\Delta(W / L)}{W / L} \qquad\qquad (7.24)$$

25

The widths are found from equations (7.23) and (7.24). This completes a first pass of The design. Next the simulation program is utilized. In the simulation transconductance verses voltage and transistor channel widths are optimized to yield the targeted

30   flatness.

In an alternative embodiment, a high degree of linearity is not be necessary. Ripple is allowed in the transconductance curve to produce satisfactory linearity.

In an embodiment the maximally flat transconductance curve

35   for small signals zero IM3 distortion is produced. However, if

the curve must be maximally flat, the range of values for V_{in} is reduced. In the alternative embodiment allowing some ripple in

5   the transconductance curve, allows the range of input voltage V_{in} is that produces a finite intermodulation distortion to be extended.

FIG. 31m is a graph of the transconductance curve for The exemplary differential pair amplifier that extends the input

10   voltage range by allowing ripple in the overall G_m of the amplifier. The transconductance curve for a single differential pair amplifier 3137 is compared to one of FIG. 31i that utilizes The parameters of Table I 3139. By allowing ripple in the transconductance the range of V_{in} has been extended.

15   In an embodiment a number of additional auxiliary differential pairs are added to control IM3 distortion. However, if the devices required to implement the function obtained for a given linearity are too small than the amplifier cannot be built successfully.

20   Table II compares to tone intermodulation distortions simulation results for a differential pair against a structure described in an embodiment of the invention.

25

Two Tone Intermodulation Distortion Simulation Results							
V1_peak each	40mV	50mV	100mV	200mV	250mV	300mV	350mV
Simple diff. pair	-73dB	-69.5dB	-57dB	-45dB	-41dB	-37dB	-34.5dB
New structure	-80dB	-80dB	-75dB	-73dB	-73dB	-73dB	-57dB

Table II

30

Initially, at a 40 mV peak input strength for each of two signals input to the amplifier, linearity in the embodiment is improved to -80dB. At approximately, a 100 mV input signal

35   strength, the difference in inter modulation between the prior

art structure and the embodiment of the invention approaches 20dB.   The amplifier provides a layer response up to

5   approximately a 350mV peak input signal. Extending the linear input range by approximately 12dB results in four times the signal handling capability of that available in the prior art.

The details of linearizing a CMOS differential pair are disclosed in more detail in U.S. Patent Application

10   No. 09/573,356 filed May 17, 2000, (B600:36523) entitled "System and Method for Linearizing a CMOS Differential Pair" by Haideh Khorramabadi; based on U.S. Provisional Application No. 60/136,115 filed May 26, 1999 (B600:34678), the subject of which is incorporated in this application in its entirety by

15   reference.

FIG. 32 shows a transconductance stage 3102 with an LC load 3104 that is provided with Q enhancement 3202 and Q compensation over temperature 3206. Q enhancement 3202 tends to increase the circuit Q thus, increasing the frequency selectivity of the

20   circuit.   A Q enhancement is provided by the transconductance element's G_m, 3202 connected as shown.   Addition of this transconductance element is equivalent to adding a negative resistance 3024 that is temperature dependent in parallel with R'(T). This negative resistance tends to cause cancellation of

25   the parasitic resistance thus, tending to increase the circuit Q.

The details of Q enhanced filters are disclosed in more detail in U.S. Patent Application No. 09/573,356 filed May 17, 2000(B600: 36523) entitled, "System and Method for Linearizing

30   a CMOS Differential Pair" by Haideh Khorramabadi; based on U.S. Provisional Application No. 60/136,115 filed May 26, 1999 (B600:34678), the subject matter of which is incorporated in this application in its entirety by reference. Once an improved Q is achieved it is desirable to maintain it over the range of

35

temperatures encountered in circuit operation with temperature
compensation circuitry 3206.

5   Due to a large positive temperature coefficient inductor
quality factor (Q) is proportional to temperature. As temperature
increases the resistance in the spiral increases, degrading the
Q.   The addition of transconductance from the G_m stage 3102
tends to increase the Q of the filter. However, the effects of

10   temperature on quality factor tends to cause wide gain variation
tending to need further improvement.   In an embodiment of the
invention for a temperature range from 0 to 100°C, Q and gain
vary +/- 15% in an unenhanced filter.   In an embodiment with a
Q enhanced filter, the Q and gain variation is doubled.   In

15   multiple stages of filtering used in the embodiments, over 20 db
of gain variation is thus encountered over temperature with the
Q enhanced filters.   This results in an unacceptable change in
the conversion gain of the receiver.   A further means of reducing
the variation in Q (and thus gain) over temperature is desirable

20   3206.

ACTIVE FILTER INDUCTOR Q TEMPERATURE COMPENSATION
          FIG. 33 shows a method of stabilizing inductor Q over
temperature 3206.   This method advantageously uses a DC

25   calibration loop 3202 and a dummy inductor 3304 to control the
value of inductor series resistance R(T) and a resistive element
R(1/T) 3314 to produce a net constant resistance. Thus, Q induced
variation in filter response due to temperature are controlled.
This method advantageously does not require the use of any high

30   frequency signals in the tuning process.   An inductor 3306 as
utilized in the filters of FIG. 30's filter bank 3002 with its
associated series resistance R(T) is shown as an element in a
temperature compensation circuit 3208. An electronic device that
supplies a variable resistance 3310 of an amount inversely

35   proportional to temperature is added into the circuit 3314.   The

decreasing resistance of the additional resistance 3314 with increasing temperature counteracts the increasing resistance of

5   the inductor's series resistance R(T). In the circuit diagram this decreasing resistance is shown schematically as R(1/T). This resistance is provided by the active resistance of a PMOS transistor biased accordingly 3314. However any device capable of producing the desired resistance characteristic described

10   above is an acceptable substitute.

A PMOS resistor is used in two places 3312,3314 to place the control element 3314 in the circuit and remove the control circuit 3208 from a main circuit 3308. In the embodiment shown, the PMOS transistor's gate to source connection is placed in

15   series with the spiral inductor 3306 of the LC circuit 3308 making up an active filter stage. The active filter stage is controlled from a remotely located control circuit 3208 that contains a duplicate PMOS resistor 3312 and inductor 3304. Inductor 3304 is advantageously fabricated with the same mask

20   pattern as used for inductor 3306. The control circuitry 3208 is not a part of the filter circuitry 3308 in order to prevent undesirable interactions with the radio frequency signals present in the filter. In the control circuit shown, the active resistor 3312 in series with the spiral inductor 3304 is duplicated

25   remotely from the filter circuit 3308. To communicate the control signal 3316 the gate of the PMOS resistor 3312 is coupled to the gate of the PMOS resistor in the filter 3314.

The control circuit provides a conventional constant current and a conventional constant voltage source function to maintain

30   a constant current through and voltage across the dummy spiral inductor 3304 duplicated in the control circuit. An exemplary constant current and constant voltage source is shown 3302 incorporating a dummy inductor 3304. However, any circuit that maintains a constant voltage across, and current through the

35

inductor 3304 in the control circuit 3208 is sufficient for the design.

5   As gate voltage 3316 changes to maintain the constant current and voltage across the inductor in the control circuit 3304, the gate control signal 3316 is simultaneously fed to the LC filter stage 3308 PMOS transmitter 3314 to control the resistance, and thus the Q, of the inductor in the filter circuit
10   3308.

An exemplary constant current and voltage source is illustrated 3302 comprising dummy inductor 3304. A temperature independent voltage reference V_{ref} is established by resistor R and conventional current sources I. Amplifier A's negative input
15   is connected to the voltage reference, and its positive input is connected to a symmetrical point between an identical current source and the dummy inductor. The output of amplifier A is fed into the gate of the transistor functioning as a variable resistor 3312. The constant voltage drop over temperature at the
20   node V_{ref} is compared to the voltage at the positive amplifier terminal. The amplifier controls the resistance of the PMOS transistor so that a constant current and constant voltage are maintained across the dummy inductor.

The calibration of inductor Q is described in more detail
25   in U.S. Patent Application No. 09/439,156 filed November 12, 1999 (B600:34014) entitled "Temperature Compensation for Internal Inductor Resistance" by Pieter Vorenkamp, Klaas Bult and Frank Carr; based on U.S. Provisional Application No. 60/108,459 filed November 12, 1998 (B600:33586), the subject matter of which is
30   incorporated in its entirety by reference.

COMMUNICATIONS RECEIVER

FIG. 34 is a block diagram of a communications network utilizing a receiver 3402 according to an exemplary embodiment
35   of the invention. A communications network, such as a cable TV

network 3404, capable of generating signals provides radio frequency ("RF") signals 3406 over the air waves, through a cable or other transmission medium. Such a signal is typically single ended, although differential transmission is contemplated. A receiver front end 3408 next converts the RF single ended signal to a differential signal. In the embodiment shown the front end provides low noise amplification of a weak received signal by a low noise amplifier. The embodiment shown also includes an attenuator to reduce a strong received signal's level. An externally supplied control signal 4302 controls the amount of attenuation, or gain of the RF signal. A receiver front end, or a Balun may be used to convert a single ended signal 3406 to a differential signal or vise versa 3410.

The receiver block 3402 which contains an exemplary embodiment of the invention next converts the differential radio frequency signal 3410 to a differential intermediate frequency (IF) 3412. Equivalently, single ended signals, or a mixture of differential and single ended signals are utilized in the receiver block 3402.

A large gain range high linearity, low noise MOS variable gain amplifier ("VGA")3403 is present to adjust the IF signal level 3412. A control voltage 3407 controls the gain of the IF signal such that a linear control voltage verses gain response is produced. A linearization circuit 3405 produces the linear control voltage from the control signal input 4302. The IF signal 3412 is next converted down to DC and demodulated into a base band signal 3414 by a demodulator 3416. At this point the base band signal 3414 is suitable for presentation to the video input of a television receiver, the audio inputs to a stereo, a set top box, or other such circuitry that converts the base band signal into the intended information output.

The communication system described is contemplated to provide the function described above in one or more circuit

assemblies, integrated circuits or a mixture of these implementations. In particular, the RF front end 3408 may be

5   integrated in a single chip with receiver 3402. Alternatively, the front end and receiver may be implemented as individual integrated circuits, on any suitable material such as CMOS.

In addition, the receiving system described utilizes additional exemplary embodiments that incorporate one or more

10   transmitters and one or more receivers to form a "transceiver" or "multiband transceiver." The transceiver contemplated may transmit and receive on differing frequencies or the same frequency with appropriate diplexer, transmit receive switching or functionally equivalent circuitry.

15   The frequency bands and modulation described in the specification are exemplary with the inventions not being limited in scope to any particular frequency band or modulation type.

RECEIVER FRONT END-PROGRAMABLE ATTENUATOR AND LNA

20   To achieve a low noise figure what is left out of the circuit is often as important as what is included in it to achieve a low noise figure. A circuit containing few components in desirable since each component in a circuit adds to noise generated in the circuit. Switches are often included early in

25   a signal path to switch in attenuator sections, reducing the level of a signal present. The reduction in signal level is necessary to prevent a following receiver circuit from being over driven into distortion.

In an embodiment a large gain range, high linearity, low

30   noise MOS VGA 3403 is used as an automatic gain control ("AGC") amplifier. Additionally, the circuit described as a front end circuit may also be employed as an AGC amplifier. The AGC amplifier may advantageously be used at any point in the signal processing chain where an adjustable gain and adjustable

35   attenuation according to an external control signal is desired.

In one specific embodiment, a control signal 4302 from an external pin on the integrated circuit is applied to RF front end
5   3408 and an IF AGC amplifier 3404. The control signal applied to the IF AGC amplifier 3403 is first conditioned by a linearization circuit 3405 so that a linear control of the IF AGC amplifier's gain is produced by varying the control signal 4302. The signal output by the linearization circuit 3405 is a control voltage
10   3407.

By way of example, control signal 4302 could be formed by sampling the sync pulses of the base band television signal and averaging the amplitude of the sync pulses over a period of time.

Advantageously, the present invention has eliminated the
15   need for switches, reducing a major contributor to increased noise figure.   In an integrated switchless programmable attenuator and low noise amplifier only two elements are present in the signal path to contribute to the noise figure. First an attenuator is present in the circuit path. The next element in
20   series with the attenuator in the signal path is a differential pair low noise (LNA) amplifier. In the differential pair noise figure is lowered by introducing a sufficient bias current to increase a transconductance g_m associated with the amplifier. The increased g_m decreases the noise contribution of the
25   differential pair.

By eliminating the need for switches it is possible to integrate the programmable attenuator and LNA onto a single CMOS integrated circuit. An additional advantage can be realized in using an integrated programmable attenuator and LNA as a "front
30   end" of an integrated receiver. A single integrated circuit can be economically fabricated on CMOS that contains an entire tuner circuit including the front end and the tuner. Alternatively, the front end and tuner circuits may be on separate interconnected substrates.

35

FIG. 35 is an illustration of the input and output
characteristics of an integrated switchless programmable
attenuator and low noise amplifier 3502. Attenuator/amplifier
3502 simulates a continuously variable potentiometer that feed
a linear amplifier. As the potentiometer setting changes the
signal level at the input to the amplifier changes, and the
output of the amplifier changes accordingly. The exemplary
embodiment is a two radio frequency (RF) port device--the input
port 3504 is configured to receive a single ended input signal
from a source 3508 and the output port 3506 is configured to
present a differential signal. In the single ended input
configuration one terminal upon which a signal is carried is
above ground reference 3510. In the differential output
configuration the signal is divided and carried on two terminals
above ground reference 3510.

In the exemplary embodiment multiple control signals 3512
are applied to the integrated switchless attenuator and LNA 3502.
For example these signals are used to program the attenuator to
various levels of attenuation, and for an output smoothness
control.

In the exemplary embodiment the differential output 3506
advantageously tends to provide noise rejection. In a
differential output configuration, the signal at one terminal is
180° out of phase from the signal at the other terminal and both
signals are of substantially equal amplitude. Differential
signals have the advantage that noise that is injected on either
terminal tends to be canceled when the signal is converted back
to a single ended signal. Such common mode noise is typically
of equal amplitude on each pin and is typically caused by
radiation into the circuit from external sources, or it is often
generated in the circuit substrate itself. Advantageously, the
present invention uses differential signal transmission at its
output. It should be noted that in alternate embodiments of the

invention, that a signal ended output can be produced from the differential signal by various techniques known in the art.

5   Also, equivalently a differential input may be substituted for the single ended input shown.

FIG. 36 is a functional block diagram of the integrated switchless programmable attenuator and low noise amplifier circuit. This embodiment illustrates how it is possible to

10   eliminate switches that would be required in a conventional attenuator and LNA.

A resistive attenuator 3601 is configured as a ladder circuit made up of resistors configured as multiple pi sections 3602. A method of selecting resistor values such that a constant

15   impedance is presented to the signal source is accomplished as is conventionally known in the art. An exemplary embodiment utilizes an R/2R configuration. Each pi section 3602 of the attenuator 3601 is connected to one input to a differential pair amplifier 3603. The other input to amplifier 3603 is grounded.

20   The resulting attenuation produced at the output 3604 is controlled by the number of differential amplifier stages that are turned on and the degree to which they are turned on.

Individual amplifiers 3603 are turned on or off by tail-current generators 3605 associated with each stage 3603,

25   respectively. Generation of the tail currents is discussed in more detail below in connection with FIGS. 44a and 44b. In FIG. 36 a zero or one is used to indicate if the corresponding tail-current generator 3605 is turned on or off, that is whether or not a tail-current is present. For example, a zero is used

30   to show that no tail-current is present and the corresponding generator 3605 is turned off. A one represents a tail-current generator 3605 that is turned on rendering the corresponding amplifier 3603 functional. The zeroes or ones are provided by the control lines 3512 of FIG. 35 in a manner described in more

35   detail in FIG. 43. All of the individual amplifier outputs 3506

are differential.   Differential outputs 3506 are   tied in
parallel with each other.   The resulting output 3604 is the
5   parallel combination of the one or more amplifiers 3608,3610,3612
that are turned on.   In an exemplary embodiment of the circuit
55 amplifiers have been implemented, with various combinations
turned on successively.   By using tail currents to selectively
turn amplifiers 3603 on and off, the use of switches is avoided.

10   In this configuration any combination of amplifiers 3603
could be turned on or off to achieve a given attenuation before
amplification of the signal. However, in a exemplary embodiment
of the circuit, adjacent pairs of amplifiers are turned on and
off.   Groupings of amplifiers in the on state can be of any
15   number.   In an embodiment ten contiguous amplifiers are turned
on.   The attenuation is adjusted up or down by turning an
amplifier tail current off at one end of a chain of amplifiers,
and on at the other to move the attenuation in the desired
direction.   The exemplary circuit is controlled such that a group
20   of amplifiers that are turned on slides up and down the chain
according to the control signals 3512 of FIG. 35.

Any number of amplifiers 3603 can be grouped together to
achieve the desired resolution in attenuation.   By using the
sliding configuration, input signals 3614 that are presented to
25   attenuator pi sections 3602 whose amplifiers are not turned on
do not contribute to the output signal 3604.   It can be seen from
FIG. 36 that the signal strength of the output is dependent upon
where the grouping of generators 3605 are turned on.

FIG. 37 is a simplified diagram showing the connection 3702
30   of multiple attenuator sections 3602 to the output 3604.
An attenuator 3601 is made up of multiple pi sections 3602
cascaded together.   Each pi section consists of two resistances
of 2R shunted to ground, with a resistor of value R connected
between the non grounded nodes.   Tap points 3702 are available
35   at the nodes of the resistor R.   In FIG. 37 the first set of

nodes available for tap points in the first pi section would be
nodes 3706 and 3708. After cascading all of the pi sections to
5   form a ladder network, a variety of tap points are available,
these are noted as node numbers 3706-37150 in FIG. 37. A path
from the input 3614 to any of the tap points, or nodes on the
ladder network yields a known value of attenuation at the output
3604. If multiple tap points are simultaneously connected to the
10   attenuator, the resulting attenuation is the parallel combination
of each connection. The combined or average attenuation at the
output terminal can be calculated mathematically or, it can be
determined using circuit simulation techniques available in
computer analysis programs.

15   In addition it can be seen from FIG. 37 that by providing
multiple tap points on a ladder network that in effect a sliding
multiple contact action can be implemented contacting a fixed
number of contacts, for any given position of the simulated slide
3716.   The slide 3716 is implemented electronically in the
20   embodiments of the invention   The average attenuation by
contacting a fixed number of these tap points 3706-3715 will
increase as the slide or switch is moved from the left to the
right on the ladder network. For example, minimum attenuation
will be present when the slider 3716 contacts the force tap
25   points 3706,3707,3708,3709 at the far left of the ladder network
3601. The maximum attenuation will be achieved when the slider
3716 is positioned to contact tap points 3712,3713,3714,3715 at
the far right of the network. In the exemplary embodiment 4,
contacts are shown, however, in practice any number of contacts
30   may be utilized.
         Mechanical switches are noisy. Mechanical switches are also
unreliable and difficult to integrate on a semiconductor device.
Returning to FIG. 36, in order to be able to integrate a
switching function, and to eliminate mechanical parts, a
35   predetermined number of attenuator taps are switched to the

output by using tail current switching of differential amplifiers 3603,3605. The differential amplifiers have the advantage of being able to be switched electronically with low noise and reliability. The differential amplifiers also provide the opportunity to introduce a gain into the circuit thereby increasing the signal strength available at the output to produce a low noise amplification. The gain achieved depends upon the number of amplifiers switched in. By changing the values of resistance in the ladder network and also by increasing or decreasing the number of amplifier stages that are turned on, the resolution of the attenuator can be varied to suit the needs of the system that an integrated switchless programmable gain attenuator and LNA is used in.

FIG. 38 is an illustration of an exemplary embodiment showing how the attenuator 3601 can be removed from the circuit, so that only the LNAs or differential stages 3605 are connected. Reference numerals 3801 to 3816 each represent a differential amplifier 3603 and a generator 3605 in FIG. 36. In the 0 dB attenuation case shown the signal strength of the output would be equal to the gain of the parallel combination of the four amplifiers that are turned on 3801,3802,3803,3804. The four activated amplifiers are indicated by a "1" placed on the circuit diagram. In an exemplary embodiment in which the sliding tap arrangement is used such that a given number of amplifiers are always turned on the configuration of FIG. 38 is necessary such that zero decibels of attenuation can be achieved when the required number of amplifiers are always turned on.

In an exemplary embodiment according to FIG. 38, a full 14 dB gain from a combination of ten amplifiers is seen when a ten tap configuration is used with the top set to the 0 dB attenuation position. As the attenuation is "clicked" so that one amplifier at a time is switched, a 1 dB per pi section attenuator is placed in series with an amplifier, a full 1dB of

attenuation is not seen/click. In a graph of the control voltage versus attenuation curve this would be seen as a change in slope

5   after the tenth amplifier is switched in.   After the 10th amplifier is switched in the curve will show a 1dB/adjustment step.

FIG. 39 shows an exemplary attenuator circuit used to achieve 1 dB/step attenuation. Each resistive pi section 3602

10   makes up one step.   The characteristic impedance of the embodiment shown is 130 ohms. Using calculation methods well known in the art of attenuator design a pi pad having a characteristic impedance of 130 ohms may be realized utilizing series resistors R_s of 14 ohms or parallel or shunt resistors of

15   1,300 ohms R_p.

FIG.40 illustrates an exemplary embodiment of an attenuator for achieving a finer resolution in attenuation.   In this embodiment a resolution of .04 dB/tap is achieved.   In the embodiment shown each series resistor R_s, connected between the

20   shunt resistors in the ladder network has a string of series resistors connected in parallel with it.   Each interconnection point between the added resistors 3402 provides a tap point that provides a finer adjustment in attenuation values.

In implementing an integrated, switchless, programmable

25   attenuator and low noise amplifier, calculating the overall gain of a parallel combination of amplified and attenuated signals is analytically complex to calculate.   For example, consider an embodiment utilizing 10 differential pair amplifiers in the output, connected to 10 different tap points.   Ten signals

30   receiving varying attenuations are fed into individual differential pair amplifiers. Gain of the amplifiers varies according to an adjustment for monotonicity. The amplified signals are then combined in parallel to yield the output signal.

Tail currents in the differential output amplifiers are not

35   all equal.   The tail currents determine the gain of a

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differential pair, and are adjusted to provide a specific degree
of monotonicity. Thus, the gain of each of the differential pair

5   amplifiers varies across the 10 interconnected amplifier. The
attenuation varies since each tap is taken at a different point
to be fed into each of the differential amplifiers. In such an
arrangement it would be expected that the middle signal line
would represent the average, yielding an approximate figure for

10   the attenuation and gain of the combination of 10 signal lines.
However, this is not the result. Through the use of computer
simulation the behavior of this network has been simulated.
In simulating behavior of this network it is found that the first
tap predominates in defining a response from the sum of the 10

15   taps. The first tap has the least attenuation and this yields
the predominant signal characteristics.

     In an embodiment utilizing 10 sliding taps the amplifier
gain is a constant 14dB. The attenuator range is from 0-25 dB
in 1dB steps. This yields an overall range of -11 dB to +14 dB

20   for the combination of attenuator and amplifiers.

     FIG. 41 illustrates the construction of the series and
parallel resistors used an integrated attenuator. In this
embodiment all of the resistors used are 130 ohms. This is done
to control the repeatability of the resistor values during

25   fabrication. Ten of these resistors are connected in parallel
to yield the 13 ohm resistor used as the series attenuator
element R_s of FIG. 39. Ten of these 130 ohm resistors are
connected in series to yield 1,300 ohms to realize the parallel
resistance legs R_p of FIG. 39 of the attenuator. Building the

30   attenuator from unit resistors of 130 ohms also, provides
improved matching. By matching resistor values in this method
variability is minimized to that of the interconnections between
the resistors. This allows the ratio between series and parallel
resistances to remain constant from pi section to pi section 3602

35

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in the ladder network that makes up the attenuator 3601 of FIG. 36.

5 FIG. 42 is an illustration of an exemplary embodiment utilized to turn on each of the differential amplifiers. This arrangement produces a monotonically increasing output verses control voltage 4202. In this illustration, five amplifiers 4204-4208 grouped together make up the electronically sliding tap arrangement. Numbers on the illustration indicate the fractions

10 of tail-currents relative to the full value used to turn on each amplifier. Amplifiers are partially turned on at the ends of the group. Gradual turn on of the amplifiers at the ends of the group is done to control overshoots and undershoots in the amplifier gain. These over shoots and under shoots are seen upon

15 the application of a control voltage applied.

Varying a smoothness control provided in a programmable attenuator and LNA to one extreme yields good linearity in the frequency response but overshoots in gain with increases in control voltage. Varying the smoothness control to the other

20 extreme yields a very smooth gain verses control voltage curve with more nonlinearity. The optimum value for the smoothness control yields a value of monotonicity that is the maximum that the system can tolerate in the form of data loss throughout the circuit.

25 If all five amplifiers of FIG. 42 were turned on with the full value of tail-currents, the gain versus control voltage curve would be as shown in the solid line 4210. By not fully turning on some of the differential pair amplifiers the overshoot and undershoot in the gain versus control voltage curve may be

30 minimized. With the tail-currents configured on the sliding tap as shown in FIG.42, the gain versus control voltage curve will appear as shown by the dotted line 4202. In this configuration, the middle three amplifiers have their tail-currents fully turned on with the remaining two amplifiers at the beginning and end of

35 the chain only having their tail-currents half turned on.

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Equivalently, other weighing of total currents may be used to achieve substantially the same effect.

5   A plot of gain versus control voltage for the entire integrated switchless programmable attenuator and low noise amplifier would preferably appear as a staircase over the entire control voltage range. By controlling the turn on of the tail-current, the non-monotonicity of the gain versus the control

10   voltage curve is reduced so that the gain monotonically increases with the application of an increasing control voltage to yield the desired stair step shape response, where FIG. 42 illustrates one "step" 4202 in the response. Non-monotonicity in gain versus control voltage is not a time dependent phenomenon. The shape

15   of the curve tends to depends on the physical implementation of a circuit and a switching arrangement for turning tail-currents on and off.

        Non-monotonicity is an undesirable characteristic tends to degrade overall systems performance. In receiving QAM data the

20   degradation is seen as a loss in received data. By improving the monotonicity characteristic of an amplifier linearity of the amplifier is degraded. Gradual switching of the tail-currents causes some differential pairs to only partially turn on. Differential pairs that are partially turned on introduce more

25   nonlinearities into the circuit output than a fully turned on differential pair.

        A transistor that is only partially turned on is only capable of handling a smaller signal than one that is more fully turned on. A transistor that is only partially turned on

30   receiving a large input signal over drives the transistor producing a distorted output. Thus, by gradually turning on the tail-currents in some of the differential pair amplifiers, the linearity tends to be degraded, however, this degradation in linearity allows a monotonically increasing gain versus control

35   voltage curve to be achieved.

Monotonic increase of gain versus control voltage tends to improve system performance. In the case of the QAM television signal being transmitted through the amplifier a view of a QAM constellation would actually be seen to wiggle with tail-currents of all differential pair amplifiers simultaneously and fully turned on.   With gradual tail-current switching, the constellation is not seen to wiggle, and data is not lost. The problem with the non-monotonicity causing the constellation to wiggle is that each time an attenuator value is switched into the circuit QAM data tends to be lost, thus degrading overall system performance of the signal transmitted through the circuit.

As part of an exemplary embodiment's operation, an automatic gain control (AGC) 3512 of FIG. 35 would be generated as one of the control signals by external receiver circuitry to adjust the input signal level presented to the receiver. This AGC control voltage would be fed into a control voltage input 3512 to select a value of attenuation through the circuit assembly.   It is desirable to switch the attenuator such that when the attenuation is adjusted, the data is not lost due to the switching period. In an exemplary embodiment of the present invention it is necessary to switch a maximum of .04 dB per step in attenuation value.

FIG. 43 is an illustration of an embodiment showing how individual control signals 4301 used to turn on individual differential pair amplifiers are generated from a single control signal 4302. There are many ways to generate control signals to turn on the differential pair amplifiers, individual control lines may be utilized, or a digital to analog converter may be used to transform a digital address to an analog control voltage.

In the embodiment of FIG. 43 to generate the control signals resistors 4304 are connected in series between a power supply voltage and ground to create a series of reference voltages at each interconnecting node. The voltages at each node between the

resistors is the reference input for one of a series of comparators 4306. The reference input of the comparator connects to a node providing the reference voltage setting. The other input of the comparator is connected to the control voltage 4302. When the value of the control voltage exceeds that of the reference voltage for a given comparator the comparator goes from a zero state to a one state at its output. The zero state is typically zero volts and the one state is typically some voltage above zero. The voltage generated to produce the logic one state is such that when applied to a gate of a transistor making up the current tail 4308 it is sufficient to turn on the differential pair of amplifiers that constitute the low noise amplifier (LNA) controlled by that current tail.

As can be seen from FIG. 43, all the LNA amplifiers set to be activated with a control voltage of the current setting will be turned on. In this arrangement simply increasing the control voltage simply turns on more LNA amplifier stages. Additional circuitry is required to deactivate previously activated amplifiers such that only a fixed number of amplifiers remain turned on as the control voltage increases. This is done so that the sliding potentiometer function can be implemented with this circuit.

FIGS. 44a and 44b illustrate an embodiment of one of the individual comparator stages 4308 of FIG. 43 used to turn on or off individual LNA amplifier stages. In the integrated switchless programmable attenuator and low noise amplifier the circuitry used to activate individual cells is duplicated at each attenuator's tap point and interconnected so that a sliding tap can be simulated using a single control voltage, V_{ctr} 4302. In describing a cell's operation it is convenient to start with the control voltage 4302 that is being applied to achieve a given attenuation value.

To illustrate the comparators operation, a control voltage
is applied to each of a series of comparators, as is shown in
5   FIG. 43. The circuit of FIGS. 44a and 44b makes up one of these
comparators. FIGS. 44a and 44b show the control voltage as V_{ctr},
and the reference voltage as V_{ref}. These voltages are applied to
the gates of a differential pair of transistors (Q1 Q2). The
circuit in FIGS. 44a and 44b surrounding Q1 and Q2 functions as
10   a comparator with low gain. The gain of the comparator is kept
low to control the speed of switching on and off the
tail-currents of the low noise amplifiers.

In FIGS. 44a and 44b when the control voltage input V_{ctr}
passes the reference level set at V_{ref} the amplifier with its
15   reference set closest to, but less than V_{ctr} remains deactivated.
(The n+1 amplifiers where V_{ctr} has not exceeded V_{ref} remain turned
off, until activated by V_{ctr}.) First the comparator output
"current (cell n)" goes high. When "current (cell n)", which is
connected to the gate of Q15, goes high it switches the
20   transistor on. Transistors Q16 and Q17 are used to deactivate
the adjoining current mirror circuit. Amplifier, Amp_n is turned
off by shunting current away from the current mirror 4402,
shutting off the tail current Q15. Thus, the current amplifier
cell with a comparator that has just been tripped remains turned
25   off.

Comparator output signal "next (cell n+10)" is the opposite
state of "Current (cell n)". The next 10 cells are turned on by
the control signal "next (cell n+10)". These cells have not yet
had their comparators tripped by the control voltage present on
30   their inputs. Thus the bottom of the sliding tap is pushed up
and down by the control voltage, V_{ctr}. In this state transistors
Q16 and Q17 in the next 10 cells are not conducting current away
from the current mirror. This allows the current tails of each
amplifier, Q15 to conduct causing amplifier Amp_n to be turned on
35   in each of the 10 cells.

Note that as a larger number of cells are grouped together, for simultaneous turn on, a larger number of differential

5   amplifier cells in the integrated switchless programmable attenuator and low noise amplifier are required to achieve the same attenuation range.

Once the control voltage has been exceeded for a given cell, the default state for all the previous amplifiers Amp_n is to be

10   turned on, unless the cell is deactivated by either Q1 or Q2 being activated.

The signal "previous (from cell n-10)" deactivates amplifier cells when it is in the high state. This signal is supplied from the previous identical comparator.

15   In FIGS. 44a and 44b, a provision for adjusting the abruptness of amplifier gain is provided. Transistors Q3 and Q10 are being used as variable resistors. These variable resistors are used to change the gain of the comparator. Varying the gain of the comparator allows the abruptness in the overall amplifier

20   gain to be controlled. Putting a high voltage on "smoothness control" causes the drain of Q5 and Q6 to be shorted together. The gain is reduced and a very gradual transition between states is provided by doing this.

A receiver front end such as previously here is described

25   in more detail in U.S. Patent Application No. 09/438,687 filed November 12, 1999 (B600:33757) entitled "Integrated Switchless Programmable Attenuator and Low Noise Amplifier" by Klaas Bult and Ramon A. Gomez; based on U.S. Provisional Application No. 60/108,210 filed November 12, 1998 (B600:33587), the subject

30   matter of which is incorporated in its entirety by reference, may be used before the fully integrated tuner architecture.

35

RECEIVER FREQUENCY PLAN AND FREQUENCY CONVERSION

Returning to FIG. 19 a block diagram illustrating the
5   exemplary frequency conversions utilized in the embodiments of
the invention. An RF signal 1906 from 50 MHz to 860 MHz that is
made up of a plurality of CATV channels is mixed 1916 down by a
first LO (LO$_1$) 1912 that ranges from 1250 MHz to 2060 MHz,
depending upon the channel tuned, to a first IF signal 1918 that
10   is centered at 1,200 MHz. This 1,200 MHz first IF signal is
passed through a first filter bank 1912 of cascaded band pass
filters to remove undesired spurious signals. The first
frequency conversion in the receiver is an up conversion to a
first intermediate frequency 1918 higher than the received RF
15   frequency 1906. The first intermediate frequency is next mixed
1932 down to a second IF 1922.

A second local oscillator signal at 925 MHz (LO$_2$) 1904, is
used to mix 1932 the first IF 1918 down to a second IF 1922
signal centered at 275 MHz. A second bank of band pass filters
20   1934 removes spurious outputs from this second IF signal 1922,
that have been generated in the first two frequency conversions.

A third frequency conversion 1924, or the second down
conversion to the third IF 1926 is accomplished with a third LO
(LO$_3$) 1930 of 231 MHz. A third filter 1936 removes any spurious
25   responses created by the third frequency conversion and any
remaining spurious responses that have escaped rejection through
the previous two filter banks. This third band pass filter 1936
may have its response centered at 36 or 44 MHz. A 44 MHz IF
produced by the 231 MHz LO is used in the United States while a
30   36 MHz IF is used in Europe. The LO$_3$ is adjusted accordingly to
produce the 36 MHz IF. The local oscillator's signals are
advantageously generated on chip in the described embodiments.
However, in alternative embodiments the receiver implementation
need not necessarily be limited to on chip frequency generation.
35   In the embodiment shown the second LO 1904 is advantageously

generated by a narrow band PLL circuit 1910 that includes a VCO
and a control circuit that tends to keep the VCO centered.

5

LOCAL OSCILLATOR RELATIONSHIP
    FIG. 45a is a block diagram illustrating the exemplary
generation of local oscillator signals utilized in the
embodiments of the invention. In the embodiment shown the local
10   oscillator circuitry is disposed upon a semiconductor substrate
4503. Equivalently the local oscillator signals may be produced
by circuitry that is not disposed upon a semiconductor substrate.
Other suitable materials are printed circuit boards comprising
ceramic, Teflon, glass epoxy, and so on. In the embodiment shown
15   the oscillator circuitry is integrated as a part of a tuner
integrated circuit on a common substrate. The frequency plan
utilized in the embodiments utilizes a pure third local
oscillator signal (LO3) 1930, created by direct synthesis 4502
that falls within the band of received signals. The first two
20   local oscillator signals ("LO1") 1902, ("LO2") 1904 are generated
using indirect synthesis techniques utilizing a pair of phase
locked loops 4504,4506.
    A third local oscillator ("LO3") 4502 uses direct synthesis,
to divide the second local oscillator frequency LO2 down to
25   create the third local oscillator signal LO3 1930. The local
oscillator   signals   LO1:1902   LO2:1904   LO3:1930   utilize
differential signal transmission in transmitting the local
oscillator signals to the desired mixers 1916, 1932, 1924 of
FIG. 19 respectively. In alternative embodiments single ended
30   transmission is utilized to conduct the signals to their intended
locations.
    The indirect synthesis of the first and second LOs utilizes
a frequency reference generated by a 10 MHz crystal oscillator
5408.   The 10 MHz crystal oscillator utilizes the previously
35   disclosed differential signal transmission and a unique design

that advantageously tends to provide an extremely low phase noise
reference signal.

5   The PLLs utilize tuning methods to change frequencies, as
required when tuning a desired channel or maintaining a desired
frequency once set to a desired frequency. The first local
oscillator (LO_1) 1902 is produced by utilizing a method of wide
band tuning. The second local oscillator (LO_2) 1904 is produced

10   by narrow band tuning. The embodiments advantageously utilize
a narrow band tuning circuit and method to achieve frequency lock
in the narrow band PLL.

NARROW BAND PLL 2 AND VCO

15   FIG. 45b is a block diagram that illustrates the relation
of the VCO to the second LO generation by PLL2. Circuitry to
generate the second LO frequency of 925 MHz 1904 includes a
narrow band PLL 4506. A component of the PLL loop is a voltage
controlled oscillator ("VCO") 4532 that changes the second LO

20   frequency in response to a control signal 4533. The VCO also
operates under the control of a VCO tuning control circuit 4535.
The VCO tuning control circuit generates a set of control signals
4520 that tend to maintain an optimal range of control voltage
in the VCO that in turn tends to provide a valid frequency lock

25   state in the PLL. The VCO tuning control circuit is controlled
via external signal lines that accept external commands and
provide status indications 4510 4512 4514 4516 4518 that tend to
be useful for controlling receiver operation.
           FIG. 45c is a block diagram of an embodiment of a VCO 4532

30   utilizing a tuning control circuit 4535. A control voltage 4533
acts on the VCO circuit 4532 to produce an output frequency 1904.
In the VCO circuit an increasing control voltage typically
produces an increasing output signal frequency f_{OUT}. The control
voltage typically provides a fine resolution in setting the VCO

35   frequency. The fine setting is susceptible to disruption due to

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temperature and process variations typical in VCO implementations. Typically a predetermined control voltage
5   designed to fall near the middle of a VCO's tuning range places the VCO at the center of a tuning range. It is desirable to have a VCO that tends to have a linear relationship between control voltage 4533 and frequency output 1904. However, a linear relationship tends to be difficult to maintain, especially in an
10   integrated circuit.

In an integrated circuit, process variations and temperature effects tend to work against maintaining the linear relationship. It is desirable to provide a VCO having performance that tends to be immune to these effects. A sliding window function that is
15   capable of tracking variations in circuit performance is provided by a VCO tuning control circuit 4535. The sliding function is provided by changing a VCO tank circuit's resonant frequency by varying its capacitance.

A VCO that tunes linearly at one temperature may fail to
20   maintain linearity at an elevated temperature. Likewise, a linearly tuning VCO fabricated in one lot run may be found to tune non-linearly when produced in a subsequent production run. Temperature and process effects may also cause a controlled voltage range to produce a range of output frequencies at f_{OUT}
25   that are outside of a desired tuning range. A VCO integrated onto a semiconductor substrate 4503 tends to require an improved phase noise specification over a particular tuning range.

In an exemplary PLL, with a lock range of 922 MHz to 929 MHz, suitable for use in a cable tuner disposed on a CMOS
30   integrated circuit substrate, a phase noise specification sufficient for NTSC and QAM reception tends to be desirable.

To counteract temperature in process variations in an integrated VCO, the tuning control circuit 4535 is utilized. In an embodiment the tuning control circuit 4535 is disposed upon
35   the same substrate 4503 as an integrated VCO 4532. In an

alternative embodiment the tuning control circuit 4535 is implemented off of the substrate.

5   The tuning control circuit has multiple inputs. It is supplied with a "clock" input 4514 to provide sequencing in performing its internal operations. In the exemplary embodiment the clock signal is derived from the 10 MHz reference signal 4508 of FIG. 45a. An indication of external circuitry state 4510 is

10   input to the tuning controls circuit. The "state" signal is derived from the VCO's loop filter. A "reset" line 4512 is provided as an input to reset the internal tuning controls circuitry prior to commencement of a new tuning process cycle.

         The tuning control circuit produces an output to the VCO

15   4532 comprising one or more ("n") control lines 4520 that control VCO 4532 tuning circuitry. Such tuning circuitry may be one or more circuit component that sets the VCO tuning range. In an embodiment of the invention six control lines 4520 are provided.

         The tuning control circuit 4535 provides two additional

20   outputs.   An "in lock" output 4518 provides an external indication that a phase lock condition in the VCO has been achieved. The output labeled "done" 4516 provides an indication that the tuning control circuit has finished performing its function of centering a VCO tuning range.

25   FIG. 45d is a block diagram of an embodiment of a VCO having a tuning control circuit and showing tuning control circuit interaction with major VCO components. A typical VCO as known to those skilled in the art comprises circuitry that implements the subsystems shown in FIG. 45d. Typical VCO subsystems comprise a

30   gain block 4599, a feedback network 4505 and a summing junction 4507 that couples the amplifier output, as modified by the feedback network, to the amplifier input. These functions are often   implemented   by   circuit   components   that   poses interconnections that are not as easily identifiable as shown.

35

However, in any functioning oscillator the functional subsystem and interconnections as illustrated are present.

5   A VCO is an oscillator that produces a variable frequency output f_{OUT}, that is proportional to a control voltage input 4533. A VCO is typically integrated on an integrated circuit substrate 4503. Major components of a VCO comprise an amplifier 4599 a source of feedback, such as feedback network 4505 typically comprising a resonant tank circuit and a path to couple the feedback to the amplifier's input represented by a summing junction 4507.

        The VCO shown 4532 illustrates in block diagram form the concept that for oscillations to be sustained an energy producing element, such as amplifier 4599, provides energy to a feedback network 4505 that by virtue of its interconnections feeds back a portion of signal f_{OUT} back to the input of amplifier 4599. Feedback is typically provided by a direct connection. However, feedback is also accomplished through radiation, or a parasitic path, such as through a power supply coupling. To sustain oscillations, the feedback loop must satisfy the Barkhausen criteria at f_{out}: $G(j2\pi f_{out})H(j2\pi f_{out}) = -1$, where $G(j2\pi f_{out})$ is an amplifier transfer function and $H(j2\pi f_{out})$ is a feedback network transfer function. If Barkhausen criteria is satisfied, the oscillator will oscillate to produce an output frequency, f_{ou} 1904.

        Feedback network 4505 typically comprises frequency selective elements 4509 4511 that form a tuned circuit exhibiting resonance in parallel (as shown in FIG. 45e), series or a combination of series and parallel. Such a circuit is often referred to as a resonant tank. By varying the tuned circuit element's value contained in feedback network 4505 the output frequency of oscillation f_{out} may be varied. Variation of circuit element values is accomplished with control voltage 4533 and control lines 4520. The control lines set a frequency tuning

range and the control voltage adjusts the frequency within a frequency range set through the control lines.

5   FIG. 45e is a schematic of the feedback network 4505 that allows the frequency of oscillation to be adjusted. The feedback network comprises capacitive 4511 and inductive 4509 circuit elements having frequency dependent responses. The feedback network typically comprises multiple circuit elements to produce
10   an overall frequency response. Equivalently the feedback network is intertwined with the amplifier circuit (or gain stage)(4599 of FIG. 45d). For example, a feedback network comprising an LC tank circuit as shown in FIG. 44e will resonate at a frequency dependent upon the combined values of inductance 4509 and
15   capacitance 4511. If a variable capacitance 4515 is included, as shown, a resonant frequency may be tuned over a range of frequencies by adjusting the capacitance 4515. Alternatively, an inductor 4509 may be of the variable type to adjust the output frequency 1904. However, an adjustable capacitance 4511 is
20   typically easier to fabricate on an integrated circuit substrate than a tuned inductor 4509.

     FIG. 45f is a schematic of a feedback network that allows the frequency of oscillation to be adjusted continuously by varactor tuning. Varactors typically provide a fine tuning range
25   of adjustment in a VCO. In an embodiment a continuously adjustable capacitance is provided by varactor diodes 4515. A varactor diode is a diode that poses a varying amount capacitance. The amount of capacitance depending upon a level of direct current biasing the varactor diode. To set the varactors
30   tuning range a fixed capacitance 4513 is typically used. The fixed capacitor typically gets the tuned circuit close to a desired frequency, and the varactor fine tunes the desired frequency. In an alternate embodiment a network of discreetly switched capacitors may be used in place of fixed capacitor 4513.
35   In the later described arrangement utilizing discreetly switched

capacitors, discrete ranges of tunable frequencies, with each range being continuously tunable is provided.

5   With discrete capacitor tuning it is desirable to select the value of capacitance by electronically adding or removing a capacitor, without mechanical switching. With electronic switching of capacitor values a resonant center frequency for the network is defined by one or more capacitances that are switched
10   in, combined with the capacitance as set by the varactor's current bias voltage. The capacitance range of the varactor sets the tuning range of the feedback network.

The varactors in the embodiments of the VCO are fabricated from NMOS transistors 4517. The feedback network 4505 shown
15   provides a tuning range defined by a series combination of capacitance provided by one or more varactors 4515 combined in parallel with a fixed capacitor 4513. The varactors provide a capacitance that is variable in response to a biasing control voltage 4533 applied. The varactors are disposed such that when
20   a control voltage 4533 is applied to a varactor diode, it is back biased and no current flows. In an embodiment appropriate DC blocking capacitors may be utilized to prevent current flow from the control voltage line 4533.

A varactor is typically constructed as a diode having two
25   leads. However, a discrete device package is incompatible with integrated circuit construction. In an integrated circuit a varactor may be compactly constructed from an NMOS transistor.

In the embodiments a varactor diode is constructed by shorting a drain ("D") and a source ("S") leads (or terminals)
30   of an NMOS transistor 4517. The coupled drain and source form one terminal of the varactor, and the gate forms a second terminal of the varactor. By shorting the drain and source leads of an NMOS device 4517 a bulk resistance 4519 from drain to source is present. The bulk resistance is modeled 4519 by a parallel
35   combination of two resistors each of value R. In an NMOS

transistor current does not substantially flow from gate ("G")
to either of the drain D or source S terminals. Therefore, a
5   separation of charge or capacitance is created from the first
terminal formed by the gate to the second terminal formed by the
shorted drain and source through the parallel combination of two
resistors R. A DC voltage applied to the NMOS varactor produces
a variable capacitance that is inversely proportional to the
10   applied DC voltage.

NMOS transistors are a type of MOSFET transistor, which in
turn is a type of field effect transistor, or FET. Equivalently,
other types of FETs could be utilized to form a varactor, such
as a PMOS device.

15   FIG. 45g is a graph of capacitance verses control voltage
applied to an NMOS varactor. As can be seen from this graph,
varactor capacitance 4511 tends to be inversely proportional to
an applied control voltage 4533. A portion of the curve tends
to be linear 4521. It is desirable to utilize the linear portion
20   of the tuning curve to tune the VCO. Such a curve is often
referred to as a C-V curve.

FIG. 45h is a graph illustrating average capacitance
achievable with an NMOS varactor. Here, a family of various C-V
curves are presented for different control, or source voltages.

25   Equivalent series resistance or ESR is a figure of merit for
a capacitor. The ESR of an NMOS varactor is the drain source
resistance of the shorted leads. In an exemplary design, the
NMOS FETS used to form the varactors have an atomic W/L equals
(20/0.35) that is repeated 36 times.

30   V_s is the controlled, or source voltage applied to the
shorted source and drain leads of an NMOS varactor. V_g on the
horizontal axis represents the voltage applied to the gate of an
NMOS varactor. As the gate voltage is varied from zero to a
maximum voltage, the capacitance switches between a depletion
35   capacitance ("C_{dep}") and an oxide capacitance ("C_{ox}"). The total

charge transferred during each cycle of voltage variation on the
gate, such as when a varying noise or RF signal is present in the
5   circuitry, is a measure of the effective capacitance. The
effective capacitance is represented by the area under the C-V
curve. Thus, voltage variations in the C-V switch thresholds
modifies the effective capacitance of an NMOS varactor. Thus,
flicker noise in the NMOS device tends to cause frequency
10   modulation of the VCO by changing the capacitance and in turn
changing the frequency produced by the VCO.

The capacitance produced from an NMOS connected to form a
varactor is an average value of the device's capacitance. When
the NMOS' applied gate to source voltage ("V_{gs}") is less than an
15   inherent threshold voltage ("V_t") of an NMOS transistor, the
transistor is in the "off state" and has a capacitance equal to
a depletion capacitance ("C_{dep}") of the NMOS.   This is a
relatively small value of capacitance.

When V_{gs} exceeds V_t, the NMOS is in an "inverted state" where
20   a greater oxide capacitance ("C_{ox}") is produced. A changing gate
voltage produces a capacitance that is not linear, but rather an
average capacitance.   The capacitance switches between a low
capacitance and a high capacitance value depending upon signal
swing present across the NMOS, such as is present in an RF
25   signal.

The value of average capacitance depends upon the time the
MOSFET is "inverted" compared to the time that it is "off". The
voltage gating the varactor on and off is the voltage swing
across the varactor. For example the voltage swing across the
30   varactor is the result of the VCO output's RF signal swing being
present across the varactor. Effective capacitance depends upon
a charge transfer which is equal to the area underneath the CV
curve. Thus, an integration of the area under the CV curve for
a given voltage swing ("V_g") represents the effective capacitance
35   obtained.

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Further, this average capacitance is a linear function of
the signal swing and the control voltage. As the voltage on the
source drain connection ("V_s"), which is the control node, is
changed, the switching point is changed, since the voltage on the
gate V_g must exceed the voltage on the control node by V_t before
the large oxide capacitance is formed. Thus, by changing the
control voltage V_s, the capacitance of the NMOS varactor is
changed.

FIG. 45i is a schematic of an embodiment of a VCO 4532 that
includes an amplifier 4599, a feedback network 4505 and summing
function 4507 in its circuitry. The embodiment shown utilizes
NMOS varactors 4517 to provide frequency control.

The amplifier circuit 4599 consists of a pair of NMOS driver
transistors M1 M2. The NMOS drivers each poses an inherent
capacitance C_{gs} that tends to contribute to the tuning of the VCO.

Transistor M1 has its source coupled to ground. The drain
of M1 is coupled to the gate of M2, a first terminal of a first
inductor 4509, the first terminal of a first varactor 4515 and
a set of first terminals of a first bank of six capacitors 4528.
A set of second terminals of the first bank of six capacitors are
each coupled to one of a first set of six transistor switches
4527 drains. The sources of the switching transistors are coupled
to ground. The gates of each of the switching transistors are
coupled to individual control lines b_1 through b_n 4520 that make
up the n control lines that originate from the tuning control
circuit (4535 of FIG. 45d).

Transistor M2 has its source coupled to ground. The drain
of M2 is coupled to the base of M1, a first terminal of a second
inductor 4509, the first terminal of a second varactor 4515 and
a set of first terminals of a second bank of six capacitors 4528.
A set of second terminals of the second bank of six capacitors
are each coupled to one of a second set of six transistor
switches 4527 drains. The sources of the second set of switching

transistors are coupled to ground. The gates of each of the
switching transistors are coupled to individual control lines b_1
5   through b_r 4520 that emanate from the tuning control circuit
(4535 of FIG. 45d).

The second terminals of the first and second varactors are
coupled together and to the control voltage 4533 supplied by the
tuning control circuit (4535 of FIG. 45d). The second terminals
10   of the first and second inductors are each coupled to the source
of transistor M3 of the adaptive bias circuit 4522.

The Adaptive bias circuit 4522 comprises a PMOS transistor
M3 with its drain coupled to a voltage supply V_{DD} and a first
terminal of a capacitor 4531. The second terminal of capacitor
15   4531 is coupled to the gate of M3. The gate of M3 is also coupled
to the first terminal of a resistor 4524. The second terminal of
resistor 4524 is coupled to the adaptive bias control line 4530
that is supplied by a constant G_m bias cell 4536.

Adaptive bias causes the transconductance of transistors M1
20   and M2 to remain fixed. Adaptive bias 4522 is provided by a PMOS
transistor M3 that tracks temperature and process variations by
virtue of being fabricated by common IC processing. Variations
in process and temperature create a varying voltage at the gate
of PMOS transistor M3.

25   The adaptive bias control line 4530 is coupled to the gates
of transistors M4 and M5 in the constant G_m bias cell 4536. The
constant G_m bias cell is representative of the functions needed
to implement adaptive bias and is conventionally constructed as
is known to those skilled in the art. The constant G_m bias cell
30   tends to maintain the transconductance of M6 (g_m) at a value of
1/R2 through local feedback. Current I varies with temperature
and process to ensure this. The value of R2 is scaled through an
amplifier gain. Appropriate scaling of M1 and M2 with respect to
M6, and of M3 to M5 gives a $g_{mM1/M2}=k(1/R2)=k(g_{mM3})$. Thus, a
35   constant g_m tends to be maintained in transistors M1 and M2.

In the constant G_m bias cell the drains of M5 and M4 are coupled to V_{DD}. The gate of M5 is coupled to the source of M5. The

5   source of M5 is also coupled to the drain of M7. The source of M7 is coupled to a first terminal of R2. The second terminal of R2 is coupled to ground. The source of M4 is coupled to the drain of M6 and the gate of M6. The source of M6 is coupled to ground.

Maintaining a constant transconductance in M1 and M2 assists

10   in maintaining a sliding window. The sliding window that is being maintained is the upper and lower limits of the VCO control voltage range. For the transconductance of M1 and M2 to remain constant, their V_{gs} must move in response to temperature and process variations. As V_{gs} moves, it is desired to have the

15   window move to track this change. The capacitance obtained across the varactor is dependent upon the V_{gs} of M1 and M2. Thus, if the V_{gs} of M1 and M2 changes, it is desirable to have the window change in a manner responsive to the change of the V_{gs} of M1 and M2.

20   FIG. 45j is a schematic of an equivalent circuit model of the VCO of FIG. 45i. In an embodiment, a design provides specific phase noise performance. The noise contributions is primarily due to flicker noise of the transistors, varactors, and the bias circuit.

25   In modeling an equivalent circuit as long as the tuneable capacitance is a small fraction of the fixed tank capacitance the flicker noise ("1/f") contribution of the varactors is minimal.

Up-conversion of 1/f noise is minimized by maximizing the gate threshold voltage ("V_{gt}") of M1 and M2 of FIG. 45j, and

30   making the transistors reasonably large. In making the transistors large the total gate capacitance present in the circuit is a constraint. The biasing transistor M3 of FIG. 44j is made wide and short to maximize gate area and minimize its head room impact. Headroom impact refers to the fact that to

35   reduce power consumption the inductors 4509 are not coupled

directly to V_{DD}. As the W/L ratio of M3 is reduced, a larger voltage is dropped across the drain and source terminals of M3.

5   To provide sufficient headroom in the described embodiment it is desired to maintain $V_{DS} > (V_{SG} - V_t)$. In a final effort to reduce 1/f noise, the gate of transistor M3 of FIG. 44j is filtered by a 100k OHM on chip resistor 4524 and a 0.1 μF external capacitor 4531, both of FIG 45j. The filtering ensures that noise from the

10   small bias devices does not adversely affect the overall noise performance of the VCO core shown in FIG. 44j. The low pass filter possesses a 10ms time constant that does not affect startup as the external .1 μF capacitor is initially charged through a switch having a worse case on-resistance of

15   substantially 50 OHMS. The .1 μF and 50 OHM resistance provide an acceptable time constant for circuit performance.

The small signal circuit model shown in FIG. 45k is a reasonable approximation of the VCO since the switched capacitors and varactors are designed to have a Q that is much greater than

20   the inductors. Thermal noise arising from the substrate and gate resistance is minimized through careful design and layout techniques known to those skilled in the art. The equivalent parallel resistance of the tank is 2R, where R is approximately equal to $(Q^2)r$.

25   FIG. 45k is a schematic of a tuning control circuit controlling switched capacitors tending to center a varactor tuning range. In FIG. 44l variable capacitors 4511 of FIG. 44f is represented by a single fixed capacitor 4509 and a series of switched capacitors C_1 through C_n and a continuously variable

30   capacitance provided by a pair of varactors 4515. The capacitors utilized in the circuit may be of any type including those suitable for integrated circuit fabrication. In an embodiment metal fringe capacitors are used for the switched capacitors. The parallel combination of the capacitors provides the required

35   overall capacitance C as shown in FIG. 44f. In alternative

embodiments capacitance in the tuned circuit may be made up of any number or combination of fixed capacitors and switched

5   capacitors. Capacitors C_1 through C_n are discrete capacitors that are added or removed from the tuned circuit by a field effect transistor ("FET") switch.

Each switch is activated through an individual control line that is part of a bus of control signals 4520 emanating from the

10   tuning control circuit 4535. In alternative embodiments the number of control lines may be reduced to less than one per switch by addressing a demultiplexer through a one or more multiplexed lines. The presence of a voltage on any one of the given control lines sufficient turn on the channel of the field

15   effect transistor effectively couples the capacitors 4528 to the tunable resonance circuit 4505.

FIG. 46a is a schematic of a PLL having its VCO controlled by an embodiment of the VCO tuning control circuit. A VCO tuning control circuit 4535 is provided to tune a VCO 4532 that is

20   contained in an exemplary narrow band PLL 4506 that generates an I and a Q 925 MHz local oscillator signal 1904. In the embodiment shown the local oscillator signal is a differential signal. However, in alternate embodiments a single ended signal is equivalently utilized.

25   The tuning control circuit makes use of a temperature and process dependent moving window of acceptable control voltages defined by a range of voltages that vary with temperature and process. The moving window tends to aid in optimally choosing a range of valid control voltages for the PLL that tend to aid in

30   attaining a frequency lock. The control circuit uses the moving window to center a varactor diode's (4415 of FIG. 45k) tuning range by adding or removing capacitance. Centering tends to avoid gross varactor non-linearities by causing a range of control voltage being utilized to fall on a linear operating region of

35   a C-V curve. Also, the circuit tends to mitigate dead band

conditions and tends to improve loop stability over process and temperature variations.

5   Process and temperature variations cause variations in VCO performance. Process variations refer to inconsistencies in the manufacturing process that can result in wafer-to-wafer and/or chip-to-chip differences. A VCO integrated on a chip can be up to ±20% off in its frequency range. Environmental effects

10   primarily consist of temperature. Pressure and humidity can have a second order effect on performance. Immediate calibration at power up is done to center the varactor diodes at the middle of their tuning range. This is done by switching in capacitors and monitoring loop voltage. To center the VCO's frequency tuning

15   range that is provided by the variable capacitance of the varactors, the embodiments of the invention immediately calibrate the VCO by adding or removing capacitance. Switching capacitors in or out of the circuit centers the varactor's capacitance range at the middle of the VCO's tuning range. To monitor centering

20   of the varactors a window comparator is used to evaluate the state of a control voltage that is used to tune the VCO. The window comparator determines when the control voltage is within the VCO's preferred control voltage range to improve the PLL performance.

25   The VCO tuning control circuitry 4535 controls the VCO 4532 of a conventional PLL 4506. The PLL is conventionally constructed as is shown in FIGS. 17-18. A reference divider 4610 is controlled by externally supplied frequency select lines 4608. The PLL comprises a crystal oscillator 4606 that inputs a stable

30   frequency to the programmable reference divider 4610. In the embodiment shown the crystal oscillator is constructed as shown in FIGS. 7-16. In alternative embodiments the crystal oscillator is conventionally constructed as is known by those skilled in the art. The reference divider is conventionally constructed as is

35   known by those skilled in the art. The reference divider in turn

outputs a frequency 4612 that is based upon the reference frequency to a first input of a phase detector 4614. The phase

5   detector is conventionally constructed as is known by those skilled in the art. A second input 4616 to the phase detector is a current output of the VCO 4532.

FIG. 46b illustrates a pulse train output of the phase detector. A pulse train 4620 is derived from the VCO output

10   signal 4616 and the reference oscillator signal 4608 as shown.

Returning to FIG. 46a the phases of the two phase detector inputs 4612,4616 are compared in the phase detector. A pulse train representing the phase difference is output 4620 from the phase detector and coupled to the input of a charge pump 4622.

15   The charge pump is conventionally constructed as is known by those skilled in the art. The output of the charge pump is fed into a low pass filter 4624. The output of low pass filter 4624 is fed into the control voltage input of the VCO 4618. The VCO outputs an image and quadrature signal 1904 at a frequency as set

20   by the frequency select line 4608.

The voltage controlled oscillator 4532 is conventionally constructed, and comprises a variable capacitance used to tune the output frequency. VCO 4532 additionally comprises a series of switchable capacitors utilized to center the tuning range of

25   the variable capacitance elements comprising the VCO. The switchable capacitors are controlled by signals emanating from the VCO tuning control circuitry 4535. The control signals 4520 are routed from tuning register 4630 to the VCO 4532.

The VCO tuning control circuitry 4535 utilizes a control

30   signal called "state" 4510 taken from low pass filter 4624. The voltage signal "state" 4510 is input to the positive inputs of a first LSB comparator 4634 and the positive input of a second MSB comparator 4636. The negative inputs of comparators 4634 and 4636 are coupled to DC reference voltages V1 and V2. These

35

reference voltages shift depending upon temperature and process conditions.

5   Voltages V1 and V2 are taken from a resistive divider circuit that utilizes a transistor to track process and temperature variations. A conventional voltage reference 4607 outputting voltage at level V1 is applied to a first terminal of a first resistor 4603 and the negative input of msb comparator

10   4636. A second terminal of the first resistor is coupled to a first terminal of a second resistor 4605 at node 4637. A second terminal of the second resistor 4605 defines voltage threshold V2 is coupled to a drain of a transistor M4. The drain of M4 is coupled to the negative terminal of lsb comparator 4634. A source

15   of M4 is coupled to ground, and a gate of M4 is coupled to node 4637.

        Comparator 4634 outputs signal lsb and comparator 4636 output signal msb. Voltages V1 and V2 set thresholds to form a sliding window which monitors the state of the closed PLL by

20   monitoring voltage 4510 at low pass filter 4624. Control voltage 4510 is taken as the voltage across a capacitor in the low pass filter that induces a zero in the loop filter 4624. Thus, the control voltage is a filtered version of the control voltage of the PLL loop, and thus tends to have eliminated spurious

25   components present on the VCO control line.

        Signals msb and lsb are fed in parallel to a 2 input AND gate 4640 and a two input exclusive NOR gate 4642. The output of exclusive NOR gate 4642 is fed into the D input of a DQ flip-flop 4644. The Q output of the flip-flop is fed into a two

30   input AND gate 4646, whose output is in turn fed into the clock input of a 6-bit bi-directional tuning register 4630. Returning to AND gate 4640 its output is fed into the shift left/right input port of the 6-bit bi-directional tuning register 4630.

        The reset signal 4512 is based on the output of low pass

35   filter ("LPF") 4624 and is applied to the VCO control circuit as

described below. Low pass filter 4624 takes its input from charge
pump 4622's output. A first shunt capacitor 4609 has a first
5   terminal coupled to the LPF input it has a second terminal that
is shunted to ground. Resistor 4611 has a first terminal coupled
to the LPF input and a second terminal coupled to the first
terminal of a capacitor 4613. A second terminal of capacitor 4613
is coupled to the second terminal of capacitor 4609. Transistor
10   4615 has a source coupled to ground, a drain coupled to the first
terminal of capacitor 4613, and a gate that defines a reset
signal 4512 utilized throughout the VCO control circuit. The
reset signal is coupled to an R terminal of DQ flip-flop 4644,
a reset terminal "R" of the 6-bit bi directional tuning register
15   4630, the "R" input of DQ flip-flop 4617, and a first input of
a two input OR gate 4619.

Clock signal 4514 is based on the divided reference
oscillator signal 4612. Division of the reference signal is
accomplished in any conventional manner, known by those skilled
20   in the art. Clock signal 4514 is coupled to the clock inputs of
DQ flip-flops 4644 and 4617, a clock input of the 6-bot bi-
directional tuning register 4630, and in-lock detector 4648. The
clock signal is also applied to an inverted second input of the
two input and gate 4646.

25   Threshold voltages V1 and V2 are in fixed relationship to
each other but vary in their voltage levels. The pair of voltage
thresholds, V1 and V2, utilize a MOSFET transistor M4 4635 to
provide a sliding window function. The window is formed by the
voltages V1 and V2. The actual location of the window is set by
30   the V_{gs} of MOSFET M4 since the temperature and process changes
present in M4 cause the value of V1 and V2 to change. However,
the difference in voltage between V1 and V2 remains constant.

For example, a change in temperature, the V_{gs} of M1 and M2
would change. A change in the V_{gs} of M1 and M2 causes the
35   capacitance of the varactor to change. If a window that did not

track the change of V_{gs} was not provided, then at elevated
temperature the loop would not lock. At start-up, when the chip

5   is at room temperature, V1 is set to 1.5 volts and V2 is set to
1.0 volt.   The phase lock loop will attempt to lock with a
voltage between 1.0 and 1.5 volts.   Over time, the chip
temperature increases causing the V_{gs} of M1 and M2 to change. The
capacitance changes in the varactor causes the VCO to move away

10   from the preset window. If the PLL tried to acquire lock at the
elevated temperature, it would not be able to do so within a
voltage range of 1.0 to 1.5 volts.

MOSFET M4 has the effect of making the voltages at V1 and
V2 not absolute values. However, the difference between V1 and

15   V2 remains constant and fixed. At room temperature, V1 and V2
may be 1.5 and 1.0 volt, respectively. However at 85°C, they may
drift to 2.0 and 1.5 volts, respectively. The V_{gs} of M4 changes
with the elevated temperature. The voltage at the tap point 4637
also increases with temperature forcing the position of the

20   window defined by V1 and V2 to move tracking the V_{gs} of M1 and M2.

NARROW BAND VCO TUNING

FIG. 47a is a process flow diagram illustrating the process
of tuning the VCO with an embodiment of a VCO control circuit.

25   Initially the control voltage (4510 of FIG. 46a) is evaluated to
see if it falls within a predetermined window 4702. If the
voltage is within the desired range, the time it has remained so
is determined 4704. The PLL tends to be in a state of lock when
the control voltage applied to the VCO has remained unchanged for

30   a predetermined period of time. If the voltage does not remain
in range for the predetermined time, the process is reinitiated
by looping back to the beginning. If the control voltage remains
in the range for the predetermined time, the loop is deemed in
lock, and the process is ended 4712.

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Returning to block 4702, if the control voltage is out of range a decision is made 4706 based on, wether the control voltage is above or below the desired range. If the control voltage is greater than the control voltage range, a capacitance is removed from the VCO circuit 4708. The process flow is routed to the beginning of the process, where the control voltage is again reevaluated 4702.

Returning to block 4706, if the control voltage is below the desired range a capacitor is added 4710. Next, the process routes the flow back to the beginning of the process where the control voltage is reevaluated 4702.

The VCO tuning control circuitry 4604 of FIG. 46a functions to carry out the process of FIG. 47a. If the voltage of the loop lies outside the window defined by the threshold voltages V1 and V2. The clock input to the 6-bit bi-directional tuning register 4630 is enabled. This register function may be provided by a conventional circuitry known in the art to provide this function and is not limited to the circuitry depicted. A "lock time out" circuit 4648 of FIG. 46a is reset on the rising edge of the clock signal to the 6-bit bi-directional tuning register 4630 of FIG. 46a. The "lock time out" circuit is conventionally constructed and is not limited to the components depicted in FIG. 46a.

If control voltage 4632 exceeds the upper threshold set by the comparators, zeros are shifted through the register 4630. A zero voltage decreases the capacitance in the VCO tuning circuitry by switching out a capacitance controlled by one of the 6 control lines 4628. Alternatively, any suitable number of control lines may be used other then the exemplary six. This shifting of values in a register allows one of six exemplary capacitor switch control lines to be activated or deactivated, an evaluation made and another line activated or deactivated so that the previous tuning setting is not lost. This function may

be implemented by passing a value (on or off) down a line of capacitors by shifting or by activating a capacitor associated
5   with a given line and then a next capacitor without shifting the capacitance control signal.

If the control voltage 4632 is less than the lower threshold voltage of the comparator 4634 ones are shifted through the 6-bit bi-directional tuning register.   The ones increase the
10 capacitance applied in the VCO tuning circuit by switching in a capacitance controlled by one of the 6 control lines 4628.

Once control voltage 4632 enters the predetermined valid range of operation as set by voltages V1 and V2 the shift register 4630 is disabled. At this time the locked time out
15 circuit 4648 is enabled. If the lock time out circuit remains enabled for the predetermined time period, that satisfies the in lock condition for the PLL, the clock to the DQ flip-flop 4644 is disabled, thus disengaging the control circuit. The functions described in this paragraph are constructed from standard logic
20 components known to those skilled in the art, and are not limited to those components depicted in FIG. 46a.

FIG. 47b is a flow diagram of a PLL start up and locking process for an embodiment of the invention.

A PLL start-up process is utilized to ensure that all inputs
25 to the PLL are in the proper initial state and applied at the proper time. The PLL's start-up and locking process is completed when the PLL achieves a steady state.   In the steady state condition, the PLL is set to be locked.

In response to a control signal, the PLL start-up and
30 locking process is initiated 4701.   In an embodiment, a controller utilizes a bus structure to receive data indicative of circuit performance, and to send commands to a circuit such that the coordination of circuit functions is accomplished.

After initiation of the process, the logic circuits are
35 reset 4703. Logic signals to be reset comprise a state signal

4510, and a reset signal 4512 that are inputs to the tuning control circuit 4535.

5   The next process step is directed to setting an initial VCO oscillator frequency. A tuning register 4630 is set to produce an output of all ones at process step 4705. An output of all ones causes all capacitors in the VCO to be switched into a feedback network circuit 4505 through control lines 4520 with a

10   maximum value of capacitance switched into the feedback network, the VCO is tuned to its lowest frequency where the frequency F is given by the relation,

$$F = \frac{1}{2\pi\sqrt{LC}} \qquad (7.25)$$

F = frequency in Hz (hertz)
L = inductance in H (henry)
20   C = capacitance in F (farad)

Next, the zero cap in a loop filter 5524 is zeroed in the next process step 4707.

The tuning control circuit 4535 has now been initialized and
25   VCO tuning 4709 is commenced. To tune the VCO, an MSB and an LSB signal are sampled every 64th clock cycle 4711 in an embodiment. The MSB signal is the output of comparator 4636 of FIG. 46a. The LSB signal is the output of a comparator 4634 also shown in FIG. 46. The action taken in tuning the PLL depends upon the
30   state of the MSB and LSB signals. First, an evaluation is made to determine if the MSB and LSB signals are both equal to one 4713. If the signals are both in the ones state, a capacitor is switched into the circuit 4720. The state of the circuit continues to be monitors and if the MSB and LSB are not equal to
35   one, a further evaluation is made. Next, the MSB and LSB are

evaluated to determine if both signals are equal to a zero value
4716.   If both signals are equal to the zero state, a switched
capacitor is removed 4722. The signal continues to be monitored
every 64th clock cycle 4711 and when the MSB and LSB signals are
not both equal to one or zero, a determination is made as to
whether the MSB signal is equal to zero and the LSB signal is
equal to zero 4718. If the signal does not meet this condition,
the signal continues to be monitored with the capacitance
adjusted until the MSB is equal to zero and the LSB is equal to
one for three clock cycles. Once this condition has been met,
the PLL is deemed to be in lock 4724. The circuit condition
continues to be monitored and if the PLL remains in lock for
15 reference clock cycles, the tuning circuit is disabled 4726,
and the process is ended 4728.

FIG. 47c is a graph of a family of frequency verses control
voltage for various capacitor values that illustrates the use of
comparator hysteresis to aid in achieving a frequency lock
condition. The first embodiment of the invention does not utilize
hysteresis. an alternative embodiment of the invention utilizes
hysteresis. Comparators 4656, 4634 of FIG. 46a are shown as
having hysteresis incorporated in their design. Returning to
FIG. 47c, the comparator's hysteresis about a voltage level V_L is
shown by range Δ 4730. In an embodiment, hysteresis is employed
to help achieve a PLL lock condition 4732 corresponding to a
frequency F_1 at control voltage level V_L corresponding to a tuning
capacitance value C_2.

In an alternate embodiment the utilization of a hysteresis
characteristic built into a comparator circuit aids in
maintaining phase lock. If a single fixed threshold V_1 is used,
and a lock is attempted during a temperature change, it is
possible that a phase lock condition for the loop would not be
obtainable. For example, if lock at 900 MHz is being attempted,
the circuit hunts along one of the families of curves defined by